REPORT MDC E1929

LEVEL III

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY HANDBOOK

Integrated Circuit Electromagnetic Susceptibility Investigation — Phase III

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY ST. LOUIS

MCDONNELL DOUGLAS CORPORATION

September, 1978

To: Handbook Users

Enclosed is your copy of the "Integrated Circuit Electromagnetic Susceptibility Handbook". This is the final version of the handbook, and contains your comments and suggestions from two previous versions. The handbook is expected to be a significant contribution to the EMC community. It contains information on the susceptibilities of integrated circuits to high-power RF and microwave energy. The results of literally thousands of tests of integrated circuits, including the most commonly used digital and linear types, are condensed in Chapter 4 in several easy-to-use graphs which show the lowest power levels (versus frequency) at which these circuits were observed to be susceptible. This information should be useful in a variety of EMC design and analysis activities.

While integrated circuit technology may change rapidly in the coming years, and increasingly complex circuits may appear, the information in this handbook is expected to remain an accurate estimate of the susceptibilities of future integrated circuits. The reason for this is that the present interference mechanism, rectification, is not expected to change with advances in complexity or technology. Thus, the handbook is expected to remain a valuable source for many years to come. For those interested in the basic phenomena of interference, Chapter 5 is a discussion of interference modeling. Of necessity, the discussion is rather abbreviated, but several of the references listed in this

chapter (papers from the 1978 IEEE EMC Symposium) have been reproduced and are included with the handbook for those readers desiring more information on this subject. The reprints are t-slotted, and may be inserted into your copy of the handbook, if desired, for future reference.

This year, we will hold another "Electromagnetic Susceptibility Seminar" at McDonnell Douglas Headquarters in St. Louis. The seminar will be held 25-26 October 1978. This will be the final seminar that we will hold on this subject. Two earlier seminars were very successful, and we are anticipating good attendance for this one. A tentative agenda is enclosed, as well as materials for registration, motel reservations, and for obtaining the required security clearance (out of necessity, the meeting will be classified). Please return these forms as soon as possible, if you plan to attend, to ensure your registration. We hope to see you there!

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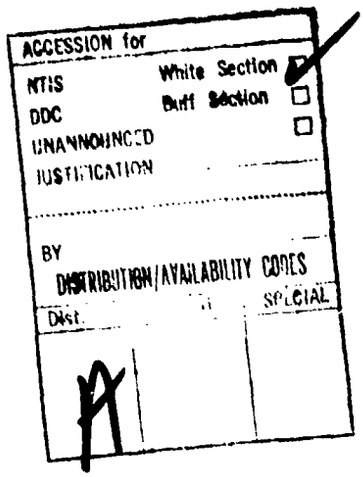

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CHAPTER 1

INTRODUCTION

The U. S. Naval Surface Weapons Center - Dahlgren Laboratory is tasked to provide electromagnetic compatibility guidance for designers of electronic systems that must operate in high power electromagnetic environments. The program involves development of technology bases on:

a. the susceptibility of integrated circuits to microwave signals,

b. the susceptibility of discrete semiconductor components to microwave signals,

c. the electromagnetic environment,

d. electromagnetic pickup (coupling) and shielding.

Each of the technology bases developed under this program will be integrated into an electromagnetic vulnerability (EMV) handbook to be published by the U. S. Naval Surface Weapons Center[1]. The EMV Handbook will assist designers in developing systems that will operate in high power RF environments, and will contain detailed information on each of the areas listed above.

The McDonnell Douglas Astronautics Company (MDAC), under contract to the U. S. Naval Surface Weapons Center - Dahlgren Laboratory, has developed the technology base on integrated circuit electromagnetic susceptibility. This document reports the information developed under this program. This is the final version of the Integrated Circuit Susceptibility Handbook; previous drafts[2,3] issued on 4 June 1976 and 3 June 1977 were widely reviewed, and suggestions and comments received from these versions have been incorporated into this final version.

The most significant information reported in this handbook is the RF and microwave power levels which are sufficient to cause interference or damage to

occur in integrated circuits. This information is the result of literally thousands of tests of integrated circuits using a computerized test setup and special test fixtures. The information has been reduced to several graphs, contained in Chapter 4, which show the minimum power levels which have been observed to cause interference or damage to occur. Integrated circuits of many different types and manufacturers were tested. The types tested include TTL and CMOS digital circuits, op amps, voltage regulators, comparators, and line drivers and receivers. Interfering signals of frequencies 220 MHz, 910 MHz, 3 GHz, 5.6 GHz, and 9.1 GHz were used in the testing. (Throughout this handbook the terms "RF" and "microwave" are used interchangeably to describe frequencies in this range). The equipment and techniques used to measure integrated circuit susceptibilities are described in the appendix.

As an example of the interference that may occur in digital integrated circuits, Figure 1.1 illustrates the output voltage of a TTL 7400 NAND gate as RF power is

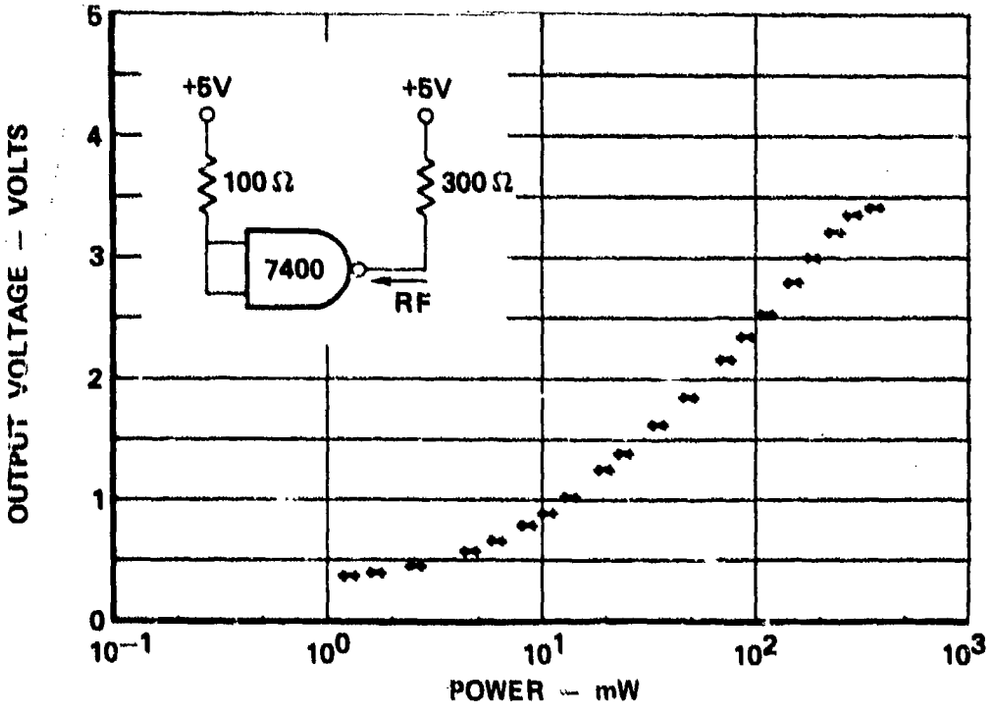


Figure 1.1. Interference in 7400 NAND Gate. RF Enters Output at 220 MHz.

conducted into the output terminal at 220 MHz. The output voltage, which is approximately 0.3 volt (a low state) in the absence of RF power, is seen to increase as RF power enters the output terminal. When the output voltage exceeds 0.8 volt, succeeding stages may not correctly recognize the low state voltage and logic errors may result. When the output voltage exceeds 2.0 volts, succeeding stages will interpret the output voltage as a high state, and logic errors are certain to occur. In this example, an RF power of 60 mW is shown to cause state errors; however, state errors have been observed to occur with as little as 9 mW of RF power.

In general, linear circuits are more sensitive to voltage offsets caused by RF energy than digital circuits, where logic states are defined in terms of voltage ranges. The interference effects generally decrease with increasing frequency of the interfering signal. As an example of interference in linear integrated circuits, Figure 1.2 shows the output voltage from ten tests of amplifiers containing 741 op amps. The circuit is an inverting amplifier with a gain of 10 and an input voltage of 0.5 volt. Microwave energy conducted into the op amp inverting input terminal at 3 GHz causes the output voltage to deviate from its

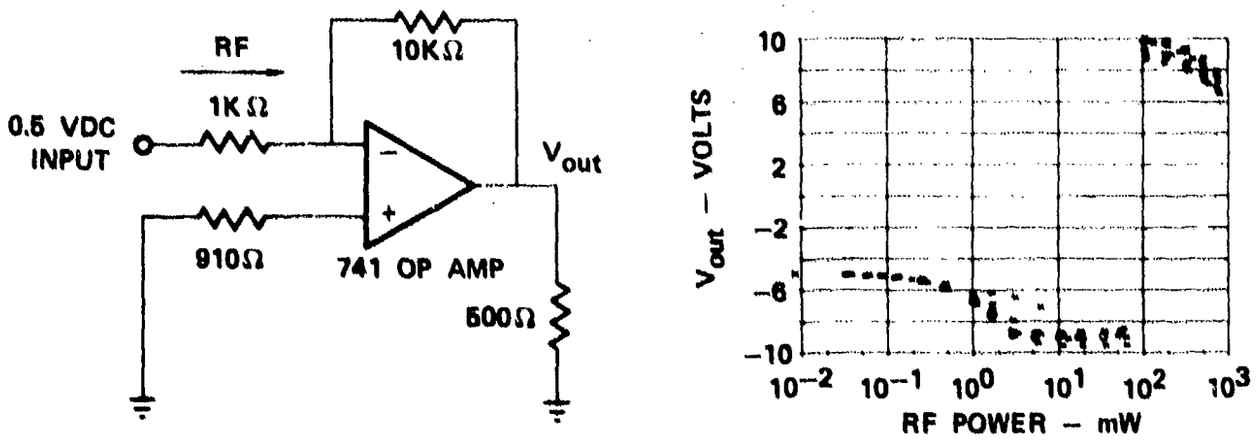
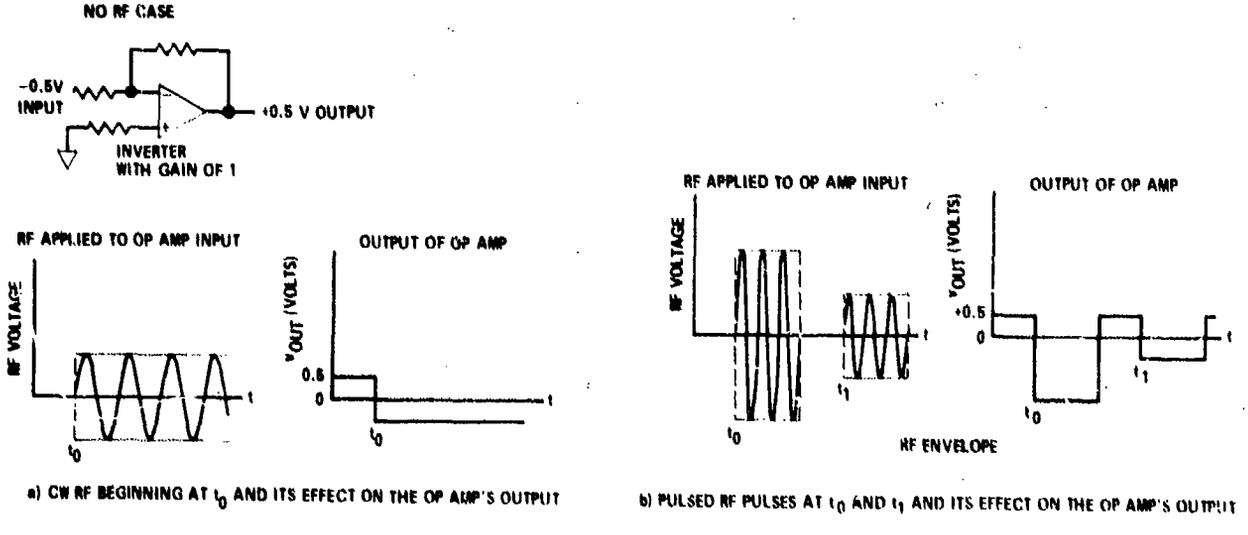


Figure 1.2. Interference in Amplifier Circuit Containing Operational Amplifier. RF Enters Inverting Input Terminal at 3.0 GHz.

normal value of -5 volts. The output voltage decreases until it saturates at -9 volts with 5 mW of RF power. Noticeable output voltage changes occur at an RF power of only 0.1 mW. It is interesting to note that at approximately 100 mW, the output voltage switches to a positive saturation voltage of about +9 volts.

If the interfering RF signal is modulated, the interference effect that is seen is also modulated. Essentially, the interfering signal is envelope detected by the semiconductor junctions in the integrated circuit. Figure 1.3 illustrates the interference that would occur in a linear circuit due to a pulsed RF signal. The circuit is an inverting amplifier with a gain of one. The input is -0.5 volt, so the expected output voltage is +0.5 volt. RF energy conducted into the op amp input terminal causes an offset voltage to appear at the op amp input which, through the feedback network, results in offsets at the amplifier output. Figure 1.3 illustrates that when the interfering signal is modulated the interference effect seen in the output voltage is modulated with the envelope of the RF signal.



a) CW RF BEGINNING AT t_0 AND ITS EFFECT ON THE OP AMP'S OUTPUT

b) PULSED RF PULSES AT t_0 AND t_1 AND ITS EFFECT ON THE OP AMP'S OUTPUT

Figure 1.3. Typical Interference Effects Due to Modulation of the Interfering RF Signal

In these examples, the interference effect was temporary and disappeared when the RF signal was removed. If the RF power level is high enough, the effect becomes permanent, or the device may not work at all. This happens when irreversible damage occurs within the integrated circuit. The effect is usually thermal in nature. Section 4.8 discusses the power levels that cause permanent damage to integrated circuits.

Since it would be difficult to measure the susceptibilities of all available integrated circuits in all possible conditions, Chapter 5 contains a brief summary of interference effects modeling. This information can be used to analyze, either qualitatively or quantitatively, interference effects in integrated circuits not specifically reported upon in Chapter 4, or under different conditions than those under which they were tested. Qualitatively, the models can help the engineer "visualize" the interference that will occur, and give him an intuitive feeling for these interference effects. Several detailed examples are presented of quantitative analyses of interference in integrated circuits using common circuit analysis computer programs. The models are well suited for worst case analyses, in which the minimum RF power expected to cause interference in a circuit is determined considering a range of possible RF conditions, and an example of a worst case analysis is included.

This handbook is intended to contain much of the information needed to estimate the susceptibility of circuits containing ICs to RF energy, and to approach the hardening task required to ensure that these circuits will operate in high power RF environments. Chapters 2, 3 and 6 supplement the device susceptibility data presented in Chapter 4 and the modeling information in Chapter 5 by presenting information on related material required to use the IC susceptibility information. Chapter 2 is concerned with electromagnetic susceptibility analysis and serves as a guide in using the information contained in the rest of the handbook. A suggested

system hardening approach is outlined, and an example of determining system hardening requirements is presented in this chapter. Chapter 3 briefly discusses coupling and shielding considerations. For conservatism and simplicity, a worst case approach is advocated to determine the maximum amount of RF power picked up from a given field. To help the designer reduce the susceptibility of circuits, Chapter 6 discusses several interference reduction techniques. Included are discussions on component screening, the use of lossy materials, and less susceptible circuit designs.

The scope of the Handbook is limited to the frequency range of 100 MHz to 40 GHz. However, the upper frequency limit of concern is actually much less than 40 GHz (closer to 10 GHz) due to two factors: the pickup of microwave energy on system cables and wiring falls off as the square of the wavelength, and component response falls off at a rapid rate due to the effects of parasitic shunt paths for the RF energy. These same two factors (i.e., pickup and component response) combine to cause concern that the RF interference problem could be more severe at frequencies less than the 100 MHz lower frequency limit used here, and to some extent it is probably so, especially for those cases where the interfering signals are "in band". While no detailed investigations of the "out-of-band" interference phenomena were carried out at frequencies less than 100 MHz, there are theoretical and practical considerations which indicate the worst case problems are adequately covered by the Handbook. In particular, the pickup on wires and cables does not approach infinity as the frequency decreases (as would be expected by extrapolating the square law dependence of the high frequency roll-off to lower frequencies) but levels off due to mismatch effects. Likewise the component responses do not continue to increase with decreasing frequency and the modeling efforts (Chapter 5) describe maximum component responses.

CHAPTER 2

ELECTROMAGNETIC SUSCEPTIBILITY ANALYSIS

The material in this chapter is intended to aid system designers and EMC engineers in using the information presented later in this handbook in developing electronic systems capable of operating in high power RF environments. The basic situation of interest throughout this chapter is illustrated in Figure 2.1. A system consisting of several electronic "black boxes" with interconnecting cables is contained within a system outer enclosure (skin). Electromagnetic radiation incident upon the system outer enclosure couples through apertures into the system interior. The internal EM fields induce RF voltages on the system interconnect cables which conduct them into the electronic "black boxes", where semiconductor devices such as integrated circuits are located. The RF voltages can be rectified by the semiconductor devices, and offset voltages and currents may be produced that are large enough to upset the operation of the electronic circuits.

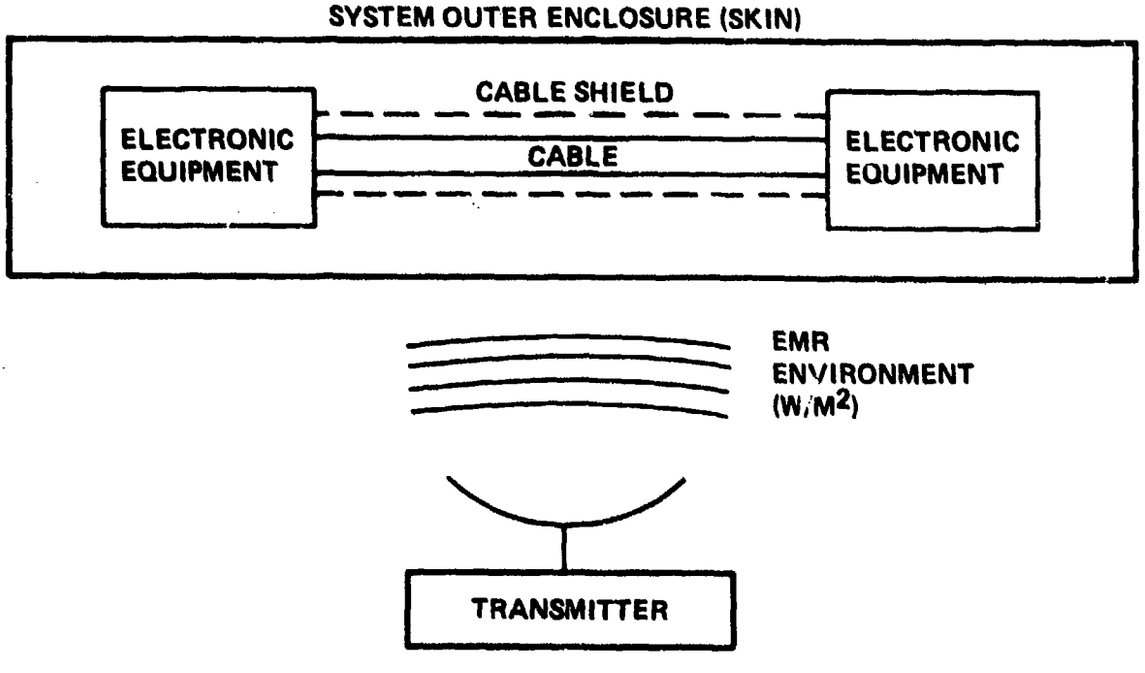


Figure 2. 1. Basic Situation of Interest. Electromagnetic Radiation Can Cause Interference in Electronic Systems.

To insure electromagnetic compatibility of electronic systems and to reduce the development time and cost of such systems, it is suggested that a well-organized hardening design plan be used. Section 1 of this chapter presents a proposed system hardening procedure to be used by system designers and EMC engineers to ensure that electronic systems will function in a given EM environment. Section 2 describes a method of determining system hardening requirements from the EM environment specifications and from information on pickup and component susceptibility. This procedure indicates how much additional hardening is required through such methods as shielding, filtering, etc., for the system to meet the given environment specification.

2.1 System EMV Hardening Approach

Figure 2.2 illustrates a proposed step-by-step system hardening task flow to ensure compatibility of electronic systems with a specified EM environment at a minimum of development time and cost. The electromagnetic environment must be known as the first step of the hardening task flow. The environment is dictated in terms of the frequencies and power densities that the system will encounter during its lifetime, including both operational and non-operational periods. Usually, the environment specification is furnished to the system designer by the customer. If this is not the case, electromagnetic environment data is available in MIL-HDBK-235[4], or measurements or analysis of the actual environment may have to be made.

The determination of pickup levels and component susceptibility can be separated into two independent tasks. The chapter on coupling and shielding (Chapter 3) gives information on determining cable pickup from environmental power density values. A worst case approach is recommended, where the maximum pickup levels by the system cables are determined. The component susceptibility chapter (Chapter 4) provides information on the minimum (worst case) power levels that cause upset in integrated circuits.

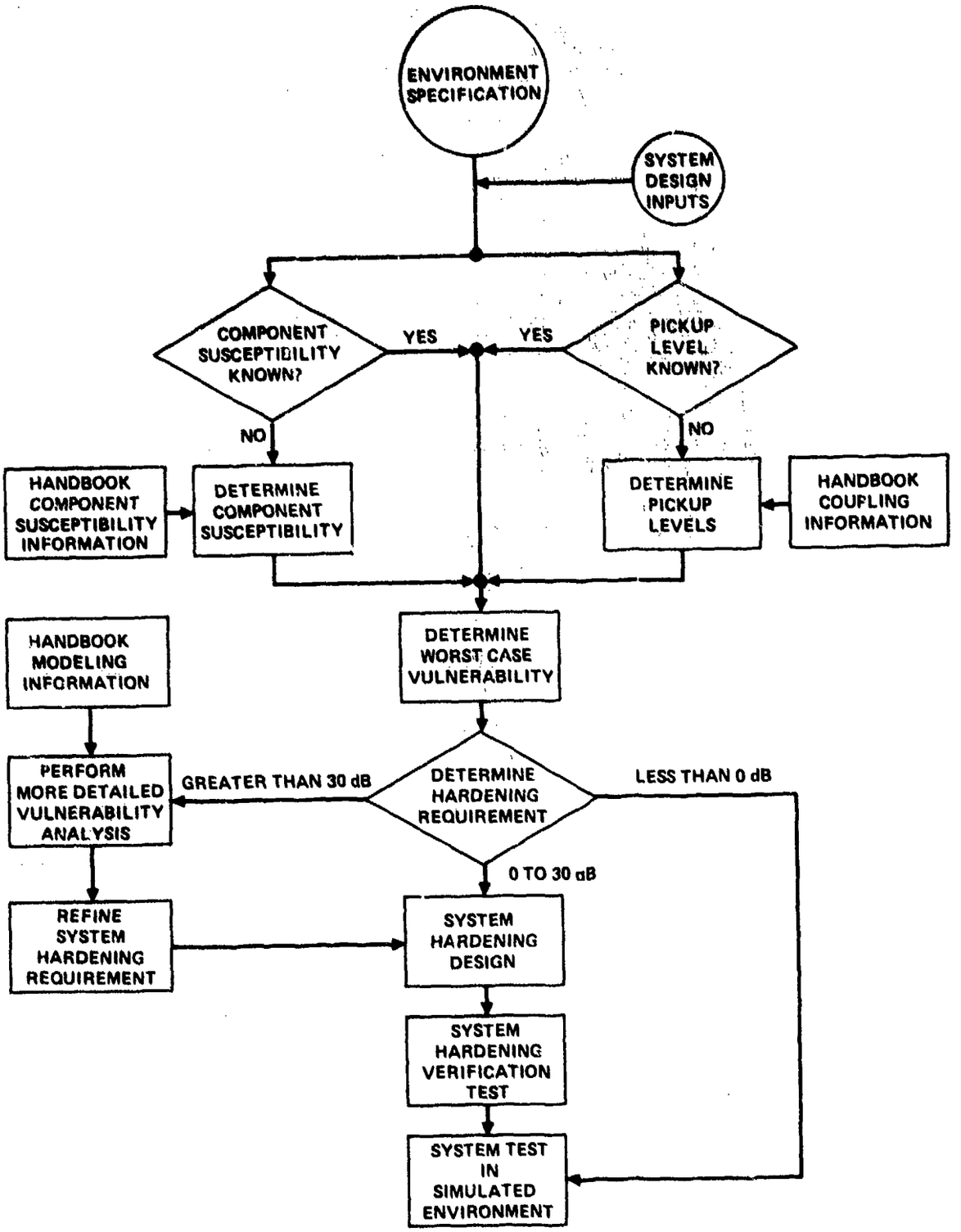


Figure 2. 2. System Hardening Task Flow

Once the pickup levels and component susceptibilities are determined, a worst case vulnerability assessment can be performed. This is done by comparing the expected maximum pickup level to the minimum power level that will cause component interference. The hardening requirement is the ratio of the maximum expected pickup level to the minimum component susceptibility level. An example of the determination of the hardening requirement is given in the next section.

Several courses of action are available to the system designer, depending on the hardening requirement determined in the previous step. If the hardening requirement is less than 0 dB, no hardening is needed and time and cost can be saved by simply proceeding to the final system test. If, however, hardening is required (indicated by a hardening requirement value greater than 0 dB), two paths are available to the system designer. If the required hardening is less than 30 dB, the most effective method is probably to proceed with the detailed hardening design. Thirty dB is a somewhat arbitrary figure: it represents a readily attainable hardening value, so that additional analysis is probably not needed. If, however, the hardening requirement is greater than 30 dB, a more detailed vulnerability analysis is probably worthwhile. This may include reassessment of the assumptions made in determining worst case vulnerability and a reassessment of the use of worst case component susceptibility data. Modeling techniques, described in Chapter 5, can be used to refine circuit susceptibility estimates. The designer may wish to consider several interference reduction options, including screening for less susceptible components and the use of less susceptible circuit designs. Also at this point the designer may isolate those portions of the system requiring more protection in separate enclosures, so that more hardening effort can be concentrated in these areas, saving cost, time and weight in obtaining the required system protection.

The system hardening design involves the choice of appropriate filters, gaskets, shielded cables, connectors, lossy materials, enclosures, etc. The hardening design also involves the integration of all of these components into the system. Tests should be performed to validate the hardening design. If possible, these should be performed so that individual hardening approaches are verified separately. For example, the shielding effectiveness of the outer enclosure can be measured without the system circuitry installed. An iterative method may be used where the hardening approach is tested to evaluate whether additional hardening is needed. If so, the hardening is added and the test repeated. After implementation of all of the individual hardening approaches, a test of the completed system should be made to verify the effectiveness of the hardening techniques.

The final step in the hardening task flow is a system test in a simulated environment to insure that the EMV specifications are met. The details of the final system test may be specified by the customer. Information on EMV tests of electronic equipment is presented in References 5, 6 and 7.

2.2 Determination of System Hardening Requirements

This section contains an example of how to calculate hardening requirements for electronic systems. Electromagnetic environment levels (in terms of power density) are determined according to the stockpile to end-of-service life cycle of the systems of interest, and a table or graph of required test levels is usually included in contractual documents. A sample environment level is shown in Figure 2.3.

The amount of power an unshielded wire or cable will pick up from this environment depends on such variables as frequency, aspect angle, terminating impedance, etc. One method for determining the maximum amount an unshielded wire will pick up is given by the formula (from Chapter 3):

$$P = 0.13\lambda^2 P_d, \qquad (2.1)$$

where P is the maximum pickup power, λ is the wavelength of interest, and P_d is the power density. Experimental data supports the use of this relationship for frequencies greater than 100 MHz (which is the lower limit of the frequencies of interest for this handbook). Using this formula, the maximum amount of power expected on system wiring can be calculated from the environment level. The resulting pickup power levels are illustrated in Figure 2.3.

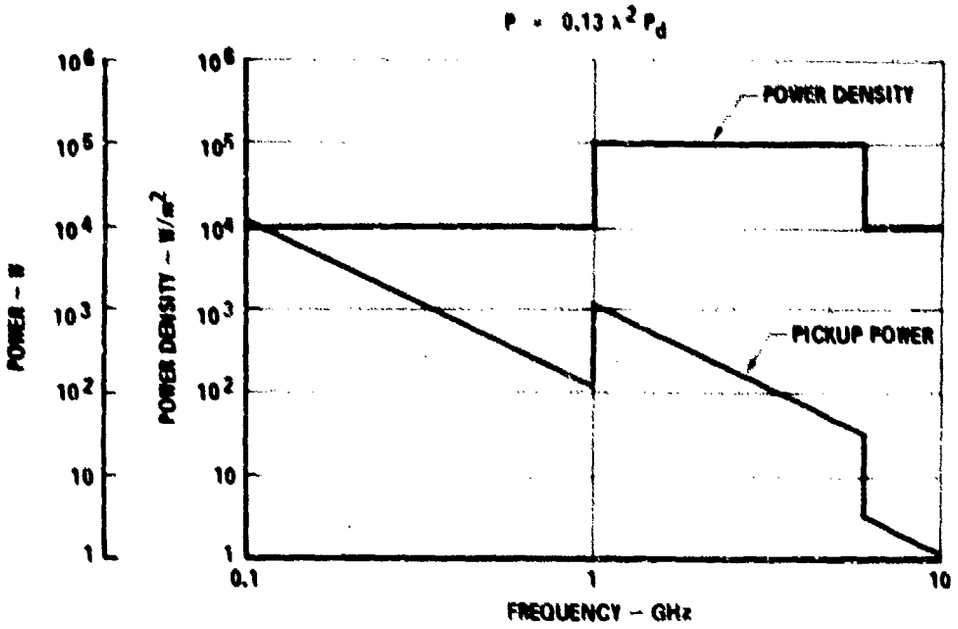


Figure 2.3. Sample Calculation of Pickup Power From Given Power Density

Figures 2.4 and 2.5 repeat the maximum power levels expected and add component susceptibility information available in Chapter 4 of this handbook. Figure 2.4 shows the worst case levels that have been observed for IC burnout (permanent damage to the circuit). The burnout levels are approximately the same for digital and linear IC's. It is clear that, in the absence of any shielding, burnout is quite possible in this example across a large frequency range, and some sort of protection in the form of shielding (either enclosure or cable, or both) or filtering is required to guarantee that component burnout will not occur. The

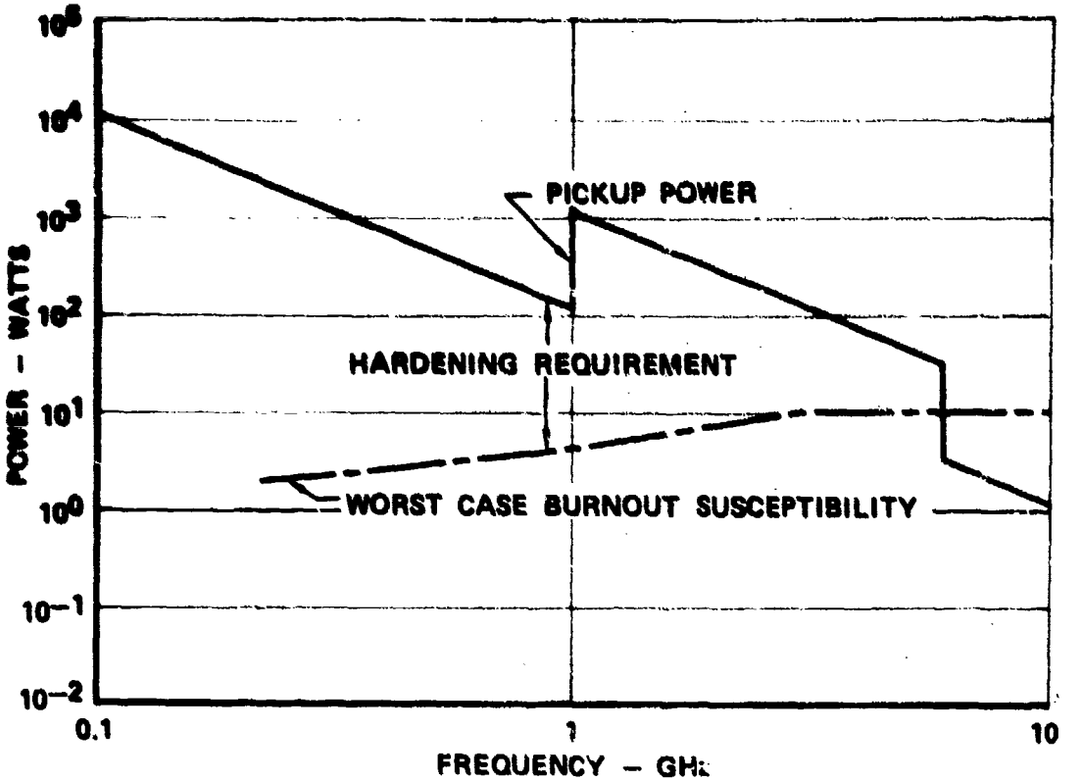


Figure 2.4. Sample Determination of Hardening Required for Burnout Protection

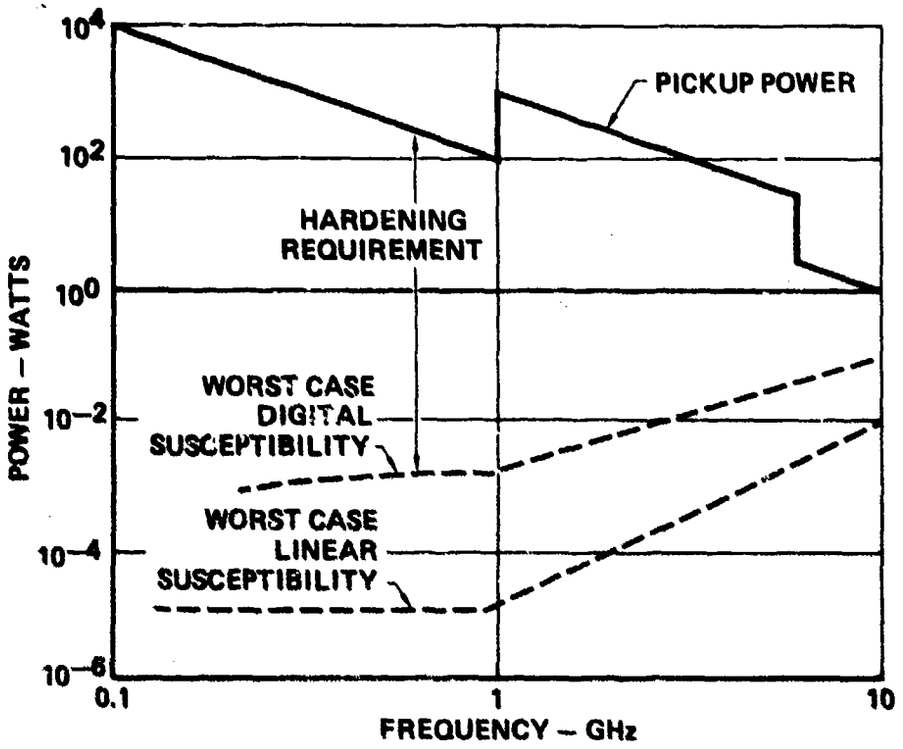


Figure 2.5. Sample Determination of Hardening Required for Interference Protection

amount of protection required is indicated by the separation of the two curves on this logarithmic plot. Figure 2.5 shows similar results for interference effects. Worst case levels observed for interference in both digital and linear integrated circuits are plotted. Digital circuits are somewhat more tolerant to interference effects than linear circuits, and Figure 2.5 shows clearly the tradeoffs, in terms of hardening requirements, involved in a choice between the two types.

The required system hardening for this example is summarized in Figure 2.6. Many options are available to meet these requirements including: splitting the shielding requirements between enclosure and cable shielding, filtering, isolation of particularly sensitive components, etc.

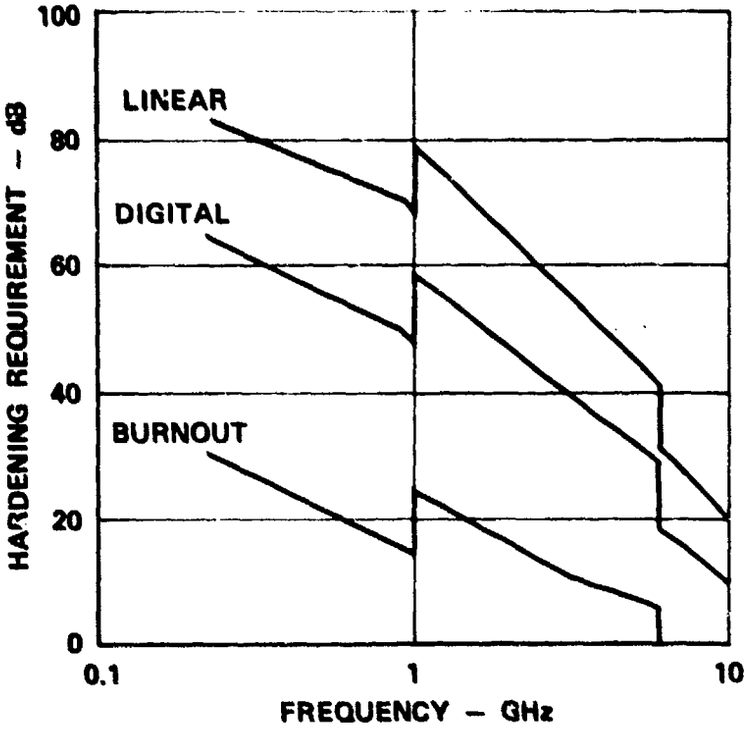


Figure 2.6. Sample Requirements for System Hardening

CHAPTER 3

COUPLING AND SHIELDING CONSIDERATIONS

This chapter briefly presents the rationale and methods for estimating worst case RFI pickup on system cables and wires for use in estimating system hardening requirements by comparison to the IC susceptibility data. The problem is divided into two parts: estimating pickup on "unshielded" cables, and accounting for inherent shielding produced by system structure, proximity of other cables, etc.

3.1 RFI Pickup on Unshielded Wires

The approach used here is to consider the interconnect wires attached to semiconductor component terminals (perhaps by way of printed circuit conductors, connectors, etc.) as generalized antennas, i.e., energy transducers which convert the radiated RF energy to conducted quantities of RF voltage and current. Predicting exact results is an immensely complicated task for all but the simplest geometries and load conditions so that a more tractable, but less precise, technique is needed.

It can be observed that the amount of power delivered to a load which terminates a typical electronic system interconnect cable in a prescribed EM field will vary greatly with changes in frequency, geometrical factors including wire routing and aspect angle relative to interfering source, and value of the terminating load. Figure 3.1 illustrates the manner in which pickup on a typical wiring specimen varies with aspect angle (the figure shows a reconstruction of the three dimensional pickup pattern as determined by different planar "slices"). Since little or no control of the relative orientation between the interference source and the victim wire bundle is available anyway, considering the aspect angle as a random variable and treatment of the pickup as a probabilistic function of the aspect angle is useful.

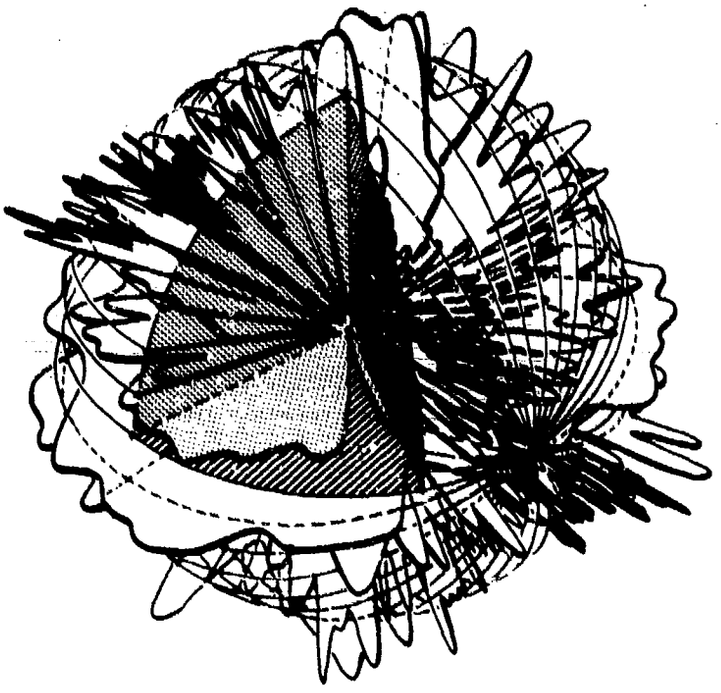


Figure 3.1. Three Dimensional Representation of Wire Pickup Pattern

Numerous measurements on representative cables[8] have shown that the power picked up in planar fields can be described by a log-normal relationship (i.e., the power measured in logarithmic units such as dBm is distributed normally) with a standard deviation between 3 and 6 dB. See Figure 3.2. Measurements using different length cables and different load impedances indicate that the measured distribution is relatively independent of such parameters (at least over the

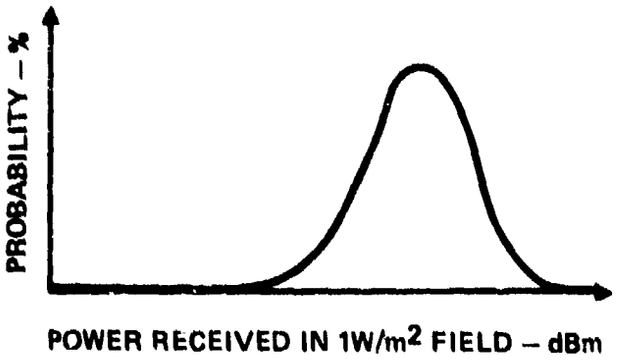


Figure 3. 2. Typical Probability Density Function for Wire Pickup Pattern

frequency range of 100 MHz to 10 GHz). Apparently, the only significant parameter is frequency (excluding shielding effects which are discussed below).

The frequency dependence is best considered from the worst-case point of view, i.e., maximum expected pickup versus frequency. To normalize results with respect to the field quantities, effective aperture is used to describe the wire pickup mechanism. Thus the measured pickup power (in watts) is divided by the incident power density (in watts per square meter) to yield effective aperture (measured in square meters). Figure 3.3 shows measured maximum effective aperture for several wire lengths, loads, and frequencies. A least square fit to the log-log plot reveals that a frequency dependence very close to inverse square results and a constrained (to f^{-2}) fit is shown superimposed on the plot. Also shown is the standard error range and the theoretical curve for a matched, half-wave dipole (effective aperture = $0.13\lambda^2$). It is clear that using the simple expression for the half-wave dipole is a reasonable upper bound for this experimental data.

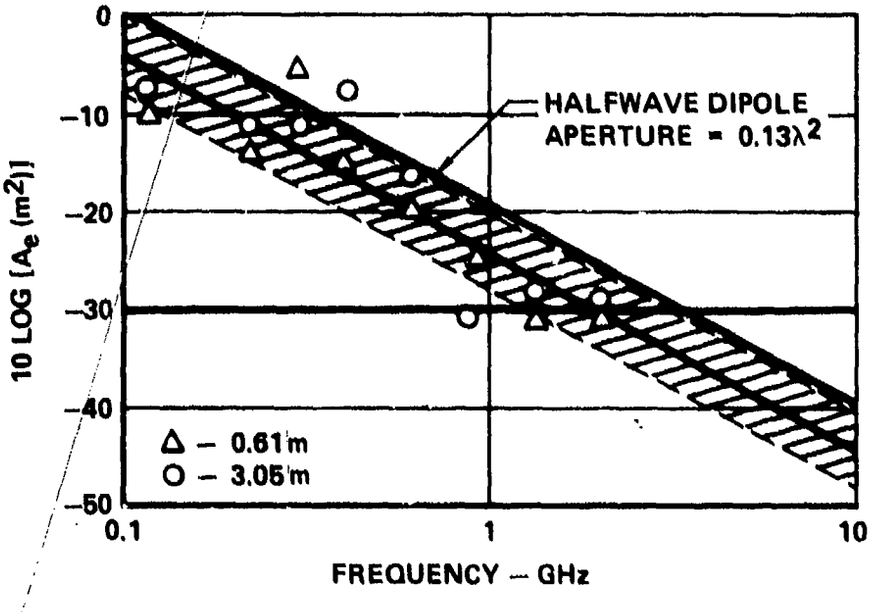


Figure 3.3. Measured Maximum Effective Apertures (A_e) of Various Wire Lengths

There are two difficulties with using the half-wave dipole expression that must be borne in mind, however. The first is that it is known that wires can be made to exhibit greater effective apertures than given by the half-wave dipole expression due to specific design and/or fortuitous focussing effects due to system structure (consider the increased pickup on a short dipole possible when a large parabolic reflector is properly located nearby). Most system configurations are not expected to produce such enhancement effects, however, so it seems unreasonable to do a worst-case system hardening design based upon such possibilities. Such possibilities strengthen the rationale for checking a system hardening design in simulated environments, though.

The second difficulty with using the half-wave dipole expression comes when it is desired to extrapolate the function to lower frequencies where the inverse square frequency dependence leads to enormous effective apertures which are not observed in practice. The paradox can be resolved by recalling that the half-wave dipole expression is for a matched half-wave dipole. The equivalent (Thevenin) driving impedance of the dipole approaches zero as the frequency approaches zero[9] so that, for a particular load on a cable, the mismatch losses counter the increasing aperture effects and the load will receive a constant amount of power, in accordance with common experience.

In summary, use of the half-wave dipole relation for effective aperture estimates in the 100 MHz to 10 GHz range is recommended for a worst case estimate of pickup in a radiated field environment, but the caveats about the probabilistic nature of the phenomena and possible focussing effects are also emphasized.

3.2 Shielding Effectiveness

The basic concept of an electromagnetic shield to be considered here is "something" that reduces the pickup on wires. Since the pickup on wires is a probabilisitc function, the concept of shielding effectiveness must be consonant

with the probabilistic description of pickup phenomena. The effects of "doing something to reduce the pickup on a wire" (i.e., "shielding" the wire) can be assessed in a manner similar to that used for "unshielded" wires. Figure 3.4 illustrates this by showing two pickup patterns (only one azimuth plane) superimposed. In general the effect of the "shield" is to reduce the pickup on the shielded wire and the quantitative description of "how much" can be derived by comparing the two probability density functions as in Figure 3.5. Experience shows[8] that the shape of the "shielded" distribution is very similar to that of the "unshielded" distribution (although this is not true for strong focussing effects which invalidate the half-wave dipole assumption) so that the difference in mean pickup and the difference in peak pickup are the same.

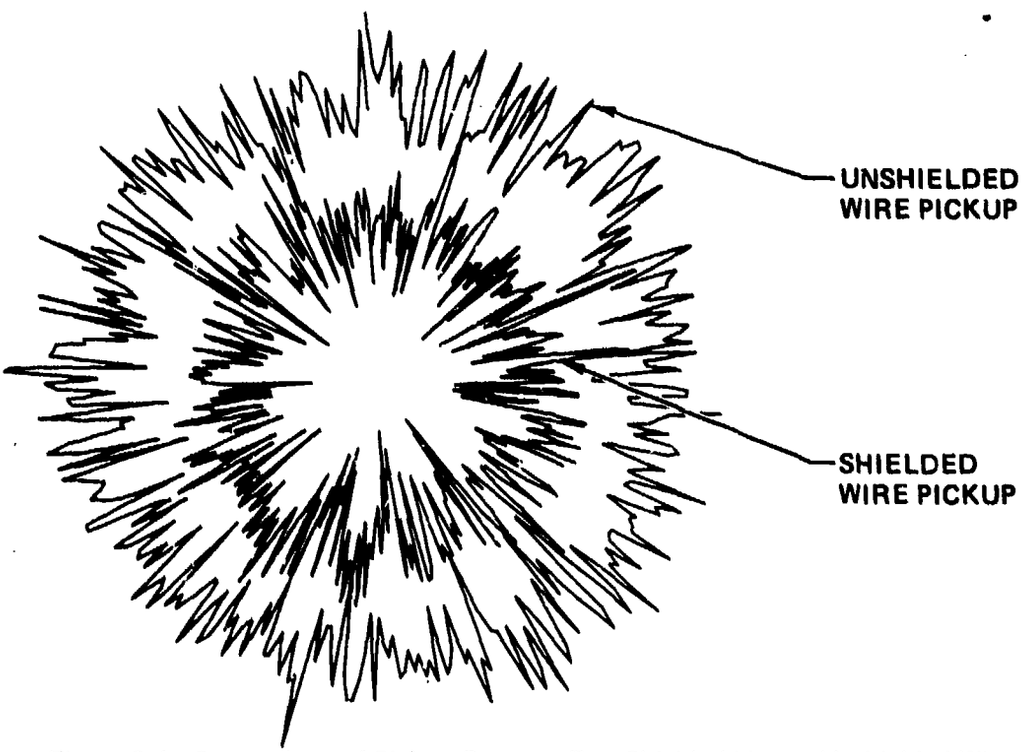


Figure 3.4. Comparison of Pickup Patterns For Shielded Versus Unshielded Wires

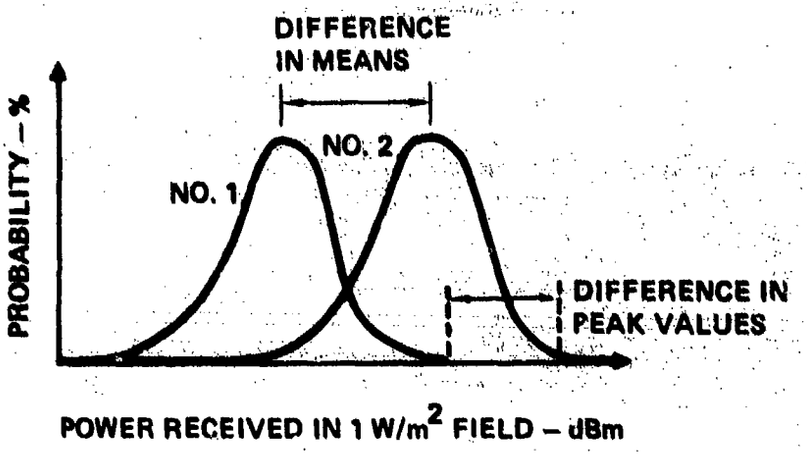


Figure 3. 5. Probability Density Functions for Shielded and Unshielded Wires

Figure 3.5 also reveals a potential trouble spot relative to the techniques used to measure the difference in pickup between a reference sample and test sample. In particular, note that it is possible to measure a larger pickup on the "shielded" sample than the "unshielded" sample. The probability of observing this condition is given by the area of the overlap in the two probability densities and, unless the curves are widely separated, this probability may be significant. The most reliable technique for assessing shielding effectiveness (short of completely determining the probability density functions) is to measure the peak pickup for each configuration. MIL-STD-1377 (Navy)[10] offers an efficient technique for accomplishing this goal over the frequency range of its applicability (generally greater than 100 MHz depending upon test chamber size).

CHAPTER 4

COMPONENT SUSCEPTIBILITY

This chapter contains information on the susceptibilities of integrated circuits to conducted RF energy which was measured in actual tests of integrated circuits during the course of this study. Literally thousands of tests were performed on integrated circuits of many different types and manufacturers. The resulting data was condensed into the graphs which are contained in this chapter. Information is included on the susceptibilities of digital circuits of the TTL and CMOS families, linear circuits including operational amplifiers, voltage regulators and comparators, and interface circuits of the line driver and receiver type. Also included is a discussion of integrated circuit package effects on the interference properties of ICs.

The device susceptibility graphs in this chapter plot the minimum RF power levels versus frequency which have been observed to cause interference to occur, as defined by some interference criterion. Where possible, measurements of the RF power absorbed by the integrated circuit were used in the estimate of the minimum RF power. In cases where measurement uncertainties cause the absorbed power measurement to be ambiguous, incident RF power measurements were used in the estimate of the minimum RF power.

Discrete frequencies of 220 MHz, 910 MHz, 3 GHz, 5.6 GHz, and 9.1 GHz were used in the testing. When measuring interference susceptibility, CW signals were used. Where pulsed or modulated signals are of interest, the pulse power or maximum envelope power should be considered in evaluating interference susceptibility. Damage susceptibility measurements were made using high power RF pulses. The damage susceptibility data is presented in terms of pulse power and pulse widths sufficient to cause damage.

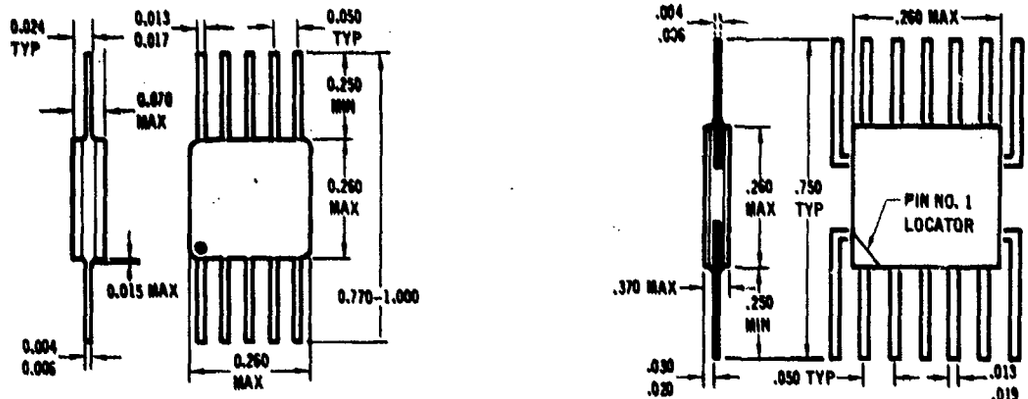
All tests and measurements reported in this chapter were made using the measuring system described in Appendix A. When tested with RF, the devices were biased as in an actual operating condition. The operating conditions for digital devices include the output state (high or low), fanout, power supply voltages, etc., while the operating conditions for linear devices include bias level, offset null settings, circuit gain, input levels, etc. For example, a TTL 7400 NAND gate is more susceptible to RF signals conducted into its output when the output state is low than when the output state is high. The effect of different operating conditions have been included in the susceptibility data reported in this chapter.

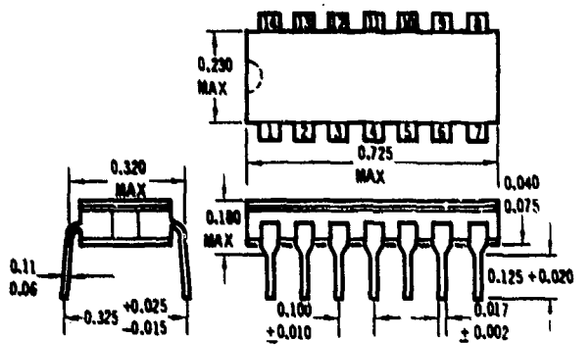
While only certain devices were tested during this study, those that were tested include several of the basic functions and common technologies. It is believed that the data in this chapter can be used to estimate the susceptibilities of many circuits that were not specifically tested. For example, modern linear ICs often contain operational amplifiers as a functional block. The susceptibility of operational amplifiers is known to be quite high (see Section 4.5), so the susceptibility of integrated circuits containing operational amplifiers is also expected to be quite high, especially if the amplifier inputs are accessible at the IC terminals (in which case the operational amplifier susceptibility data would probably be a good estimate of the susceptibility of the IC). As another example, most TTL digital devices have similar input circuits and similar output circuits. The susceptibilities of these TTL types are expected to be similar to the levels reported in Section 4.2 for those TTL devices tested in this study.

4.1 Package Effects

Integrated circuits are available in several package styles. Investigations made using some of the common IC packages revealed that no package style is superior in terms of interference reduction properties[11].

Measurements were made on the IC package types illustrated in Figure 4.1. Absorptive loss measurements were performed on TO-5 and DIP packages in which the IC chip was replaced with a shorting plate. Reflective loss measurements were performed on 7400 NAND gates in DIP and flat packages and 741 operational amplifiers





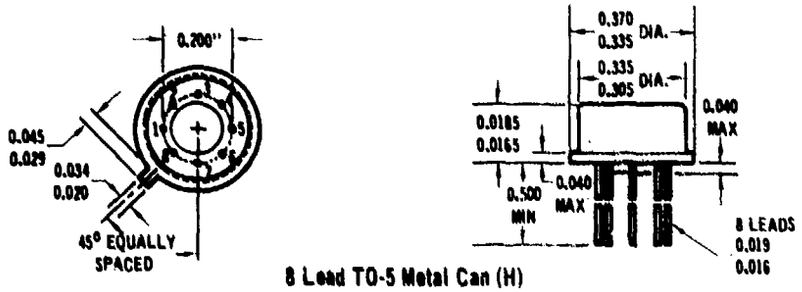


Figure 4.1. Integrated Circuit Packages

in TO-5 and flat packages. The measurement results indicate that significant differences do not exist in the absorptive and reflection loss properties of the different package styles. Therefore, the choice of package style does not appear to contribute significantly to the system hardening problem.

4.2 Interference in TTL Devices

The TTL line is the most widely used family of digital integrated circuits. Several types of TTL devices were measured to determine their minimum susceptibilities to conducted RF energy. Table 4.1 lists the specific devices tested.

Since the well-controlled RF conditions under which the devices were tested are not necessarily the same as those encountered in real-world situations, analysis was performed to determine the worst case susceptibilities of TTL circuits over the range of RF environments likely to be encountered. In particular, the RF driving impedance seen by a circuit is unknown, although a wide range of impedances is possible. The 7400 NAND gate, whose output circuitry is representative of the TTL family, was modeled for the case where RF entered the output when the output voltage was low, which was the most susceptible of the measured cases. For maximum effect, the interference was assumed to originate in a single transistor. A worst case analysis was performed over the expected range of RF driving impedances to determine

Table 4. 1. TTL Devices Tested

DEVICE NO.	DEVICE TYPE
7400	QUAD 2 INPUT NAND GATE
7402	QUAD 2 INPUT NOR GATE
7404	HEX INVERTER
7405	HEX INVERTER (OPEN COLLECTOR)
7408	QUAD 2 INPUT AND GATE
7432	QUAD 2 INPUT OR GATE
7450	EXPANDABLE DUAL 2 WIDE, 2 INPUT AND–OR–INVERT GATE
7473	DUAL J-K FLIP-FLOP
7479	DUAL D FLIP-FLOP

the minimum device susceptibilities. The models used are described in Sections 5.1 through 5.3 and the worst case analysis procedure is described in Section 5.4.

Figure 4.2 shows the worst case susceptibility values measured for the devices in Table 4.1 (solid lines) and the worst case susceptibility values predicted analytically for the 7400 NAND gate (dashed lines). Three susceptibility criteria were used to define different degrees of interference effect. The criteria were based on manufacturers' specifications for voltages in TTL circuits. The least severe interference effect, given by criterion A, is a deviation beyond the range of output voltages specified by manufacturers' data sheets. This criterion characterizes interference as a low state output voltage which exceeds 0.4 volts or a high state output voltage below 2.4 volts. The high and low state specifications are considered together because either state is possible in a digital system, and for proper logic operation both high and low states must operate correctly. RF powers greater than the susceptibility values given by criterion A do not necessarily cause malfunction of the device, but the usual 0.4 volt noise margin is reduced, so operation is risky. At RF powers below the susceptibility values given by criterion A, no interference effect will occur.

The next criterion, criterion B, is exceeded when the device low state output voltage is greater than 0.8 volts or when a high state output voltage is less than 2.0 volts. Beyond these thresholds, following stages may misinterpret the logic state, resulting in a bit error. Operation with RF powers above the susceptibility limits for criterion B is not recommended due to the high likelihood of logic state errors.

Criterion C defines the most severe interference effect. The output voltage limits for this case, low output voltage greater than 2.0 volts or high output voltage less than 0.8 volts, are the voltages at which state changes are certain. Gross errors could occur in digital systems operated at RF power levels greater

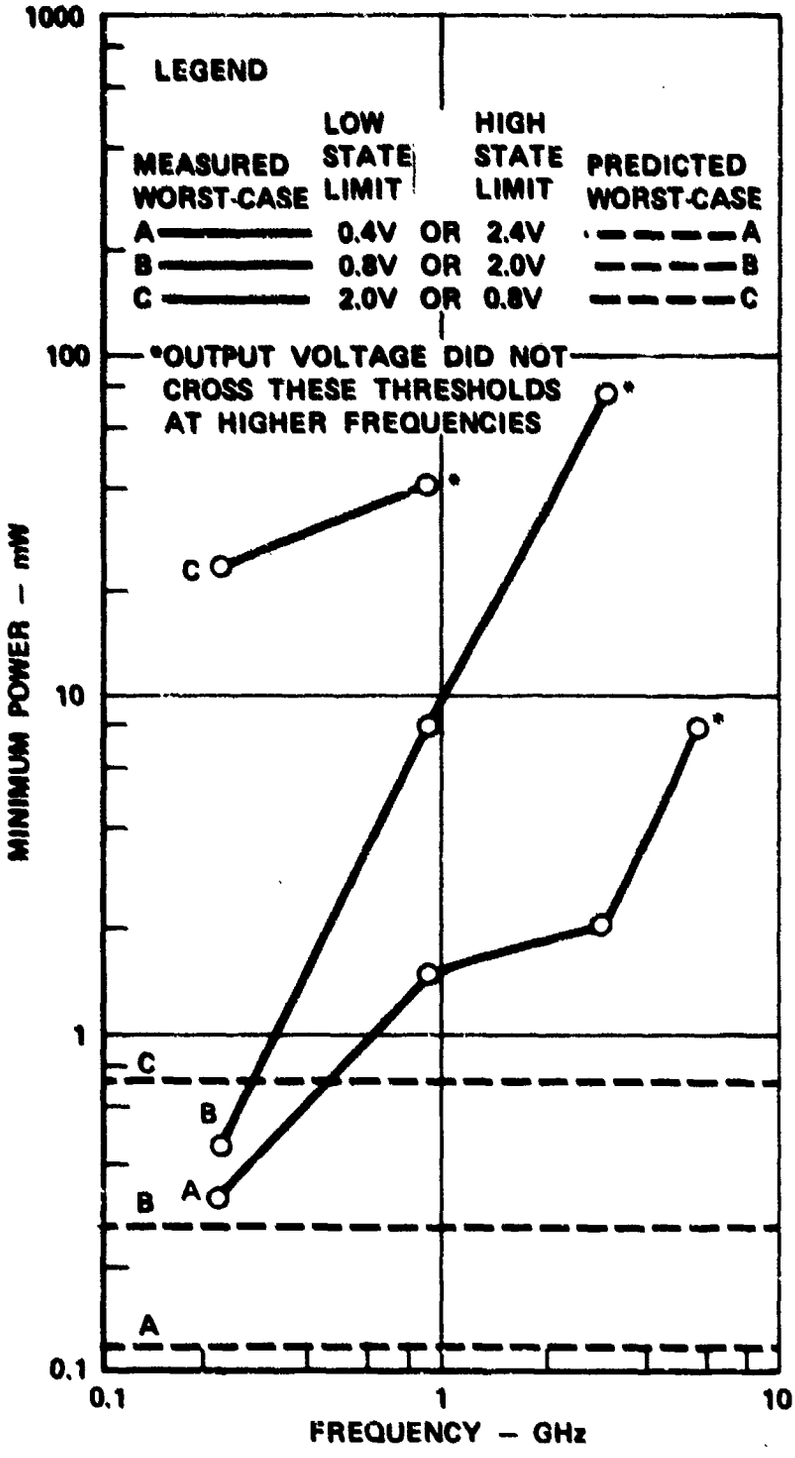


Figure 4.2. Worst Case Susceptibility Values for TTL Devices (Maximum Specification Value for Low V_{OUT} = 0.4 Volt and Minimum Specification Value for High V_{OUT} = 2.4 Volts)

than the susceptibility limits specified by criterion C.

From Figure 4.2, it can be seen that the predicted worst case susceptibilities are more conservative than the measured worst case susceptibilities. This is expected, since the analysis simulated a wider range of RF conditions than are encountered in the laboratory. The simulations included the effect of different RF driving impedances and tuning conditions, including those likely to be encountered in actual applications of electronic circuits, and assumed no external losses. It is unlikely that RF powers below these susceptibility levels will produce interference in any real-world application.

In measuring TTL susceptibility, the package supply current was also measured to determine how much RF power was required to cause significant increases in supply current. It was found that significant increases did not occur until the RF power level was far above the levels sufficient to induce state changes in the output voltage. The modeling activities also confirm this conclusion. Therefore, in TTL circuits, output voltage state changes are expected to occur before significant supply current changes are noted.

The difference in susceptibility of the low power TTL circuits (54L/74L series) and the high speed TTL circuits (54H/74H series) were also investigated. Both measurement and modeling show that the high speed devices are slightly less susceptible than the standard series (54/74), and the low power devices are slightly more susceptible than the standard series. The differences in susceptibility are small, and are probably not great enough to be significant.

4.3 Interference in CMOS Devices

CMOS digital integrated circuits are widely used in logic applications requiring low power consumption. The RF susceptibility of several types of CMOS devices were tested, including types with and without protective input diodes. Table 4.2 lists the device types tested.

Table 4. 2. CMOS Devices Tested

DEVICE NO.	DEVICE TYPE
4011A	QUAD 2 INPUT NAND GATE
4011B	QUAD 2 INPUT NAND GATE
4007A	DUAL COMPLEMENTARY PAIR PLUS INVERTER
4007B	DUAL COMPLEMENTARY PAIR PLUS INVERTER
4001A	QUAD 2 INPUT NOR GATE
4013A	DUAL "D" – TYPE FLIP-FLOP

Figure 4.3 shows the worst case susceptibility values for the devices in Table 4.2. As in the TTL case, the susceptibility criteria combine thresholds for the high and low output voltages. The threshold values used are the manufacturers' specification limits for CMOS B-series devices, or a specified difference from these specifications. The first criterion, labeled guaranteed specification limit, indicates when the output voltage is no longer within limits specified by the manufacturer. Manufacturers guarantee that the maximum low state output voltage is 0.05 volt and the minimum high state output voltage is 4.95 volts when the supply voltage is 5 volts. The devices continue to operate beyond these thresholds, but the reduced noise margin makes such operation risky. The second criterion is the edge of a 1 volt noise margin, meaning the maximum low output voltage is 1.05 volts and the minimum high output voltage is 3.95 volts. These values are guaranteed by the manufacturer to be correctly recognized by following CMOS devices. Operation outside this range is not recommended due to the high probability that logic state errors will occur. The third criterion is the most critical, defined by a 2 volt offset from the correct output voltage. The thresholds are a maximum 2 volts for the low output state and a minimum 3 volts for the high output state. Operation outside this range has a higher probability of logic state errors than the second criterion, and should be avoided.

Examination of Figure 4.3 shows CMOS devices susceptible to as little as 1 mW

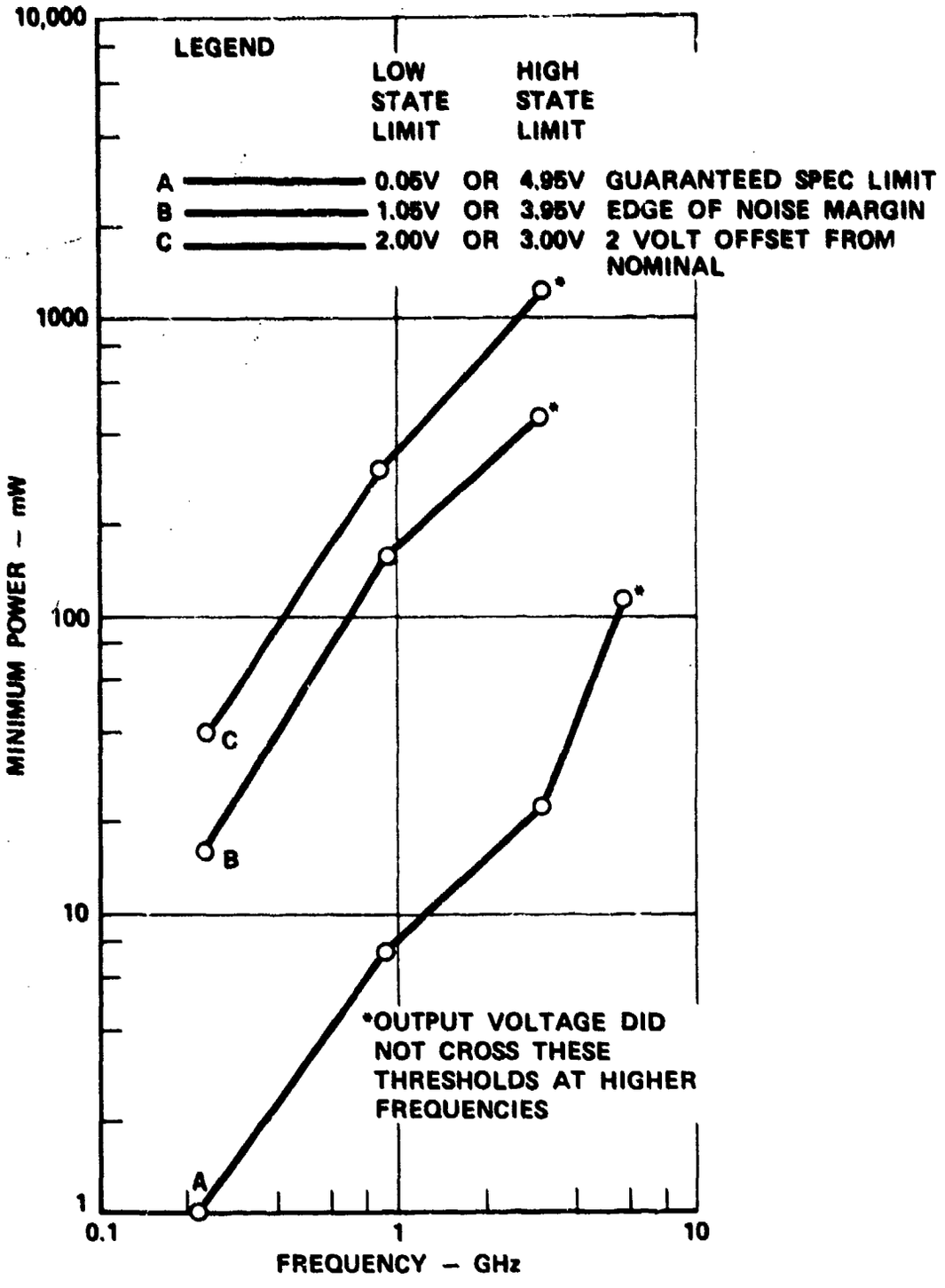


Figure 4.3. Worst Case Susceptibility Values for CMOS Devices (Maximum Specification Value for Low V_{OUT} = 0.05 Volt and Minimum Specification Value for High V_{OUT} = 4.95 Volts)

of RF power at 220 MHz. Comparison with the minimum susceptibility for TTL devices at 220 MHz shows CMOS to be approximately 5 dB less susceptible. If the noise margin is considered, CMOS appears approximately 10 dB less susceptible because of its wider noise margin than TTL.

4.4 Interference in Line Drivers and Receivers

Line drivers and receivers are often used to transmit digital data over long system interconnect cables. Long cables are potentially efficient receptors of RF energy, and the amount of RF energy conducted into the line drivers and receivers may be greater than that experienced by other components in the system. As the line drivers and receivers are located in an especially vulnerable location, special care should be taken to ensure that interference does not occur in these devices. Adequate shielding and a reduction of the data transmission rate will ensure signals of acceptable quality. The data presented in this section should enable designers to estimate the susceptibility of line driver and receiver pairs and the reduction in data rate required for quality transmission.

Table 4.3 lists the line drivers and receivers that were tested. Tests of drivers and receivers were conducted independently. The susceptibility criteria for line drivers were based on changes in the output voltage from the nominal value. Each output terminal was considered separately, and the device was considered susceptible if either output crossed the appropriate interference threshold. The

Table 4.3. Line Drivers and Receivers Tested

LINE DRIVERS	LINE RECEIVERS
8830	8820
9614	9615
55109	55107A
55110	

8830 and 9614 line drivers were tested with resistors across the output terminals simulating normal terminations. The type 55109 and 55110 line drivers have open collector (current type) outputs which were connected to pullup resistors and a +5 volt supply to give a 0 - 5 volt range for the output voltage. When the drivers were in a nominal low state, output voltage thresholds of 0.4, 0.8, and 2.0 volts defined increasing degrees of interference. When the output voltage was in a nominal high state, increasing interference was defined by 2.4, 2.0, and 0.8 volt thresholds.

For line receivers, susceptibility was defined in terms of changes in the input voltage threshold which determined the receiver switchpoint. As an example, Figure 4.4 illustrates the input-output transfer curve for a 9615 type receiver. At input voltages (differential input voltage between the two input terminals) below -0.08 volt the receiver input voltage is 5.0 volts, which is a high state output. When the input voltage is greater than -0.08 volt the output voltage is 0.2 volt,

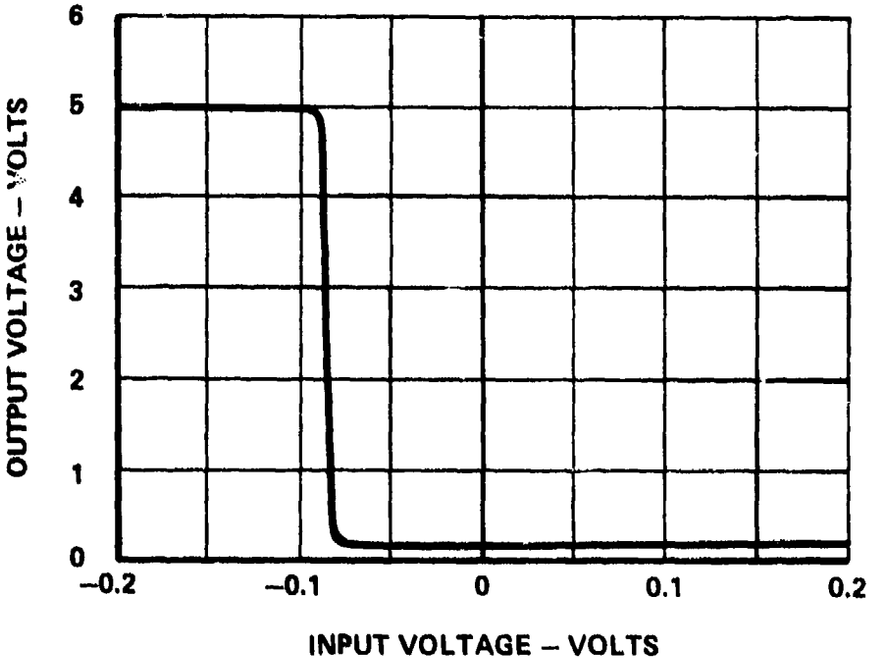


Figure 4.4. Typical Input–Output Transfer Characteristic for 9615 Line Receiver

a low state output. Thus, -0.08 volt is the input threshold voltage (V_{th}). Manufacturer specifications guarantee this threshold will be between -0.5 and +0.5 volt for this device. A threshold voltage outside this range reduces the noise margin of the device and may cause bit errors in noisy environments. Input threshold voltage changes of 0.5, 1.0, 2.0, and 5.0 volts were used for the susceptibility criteria during the testing. Threshold changes of 0.5, 1.0, and 2.0 volts represent decreasing system noise margins. A 5.0 volt threshold change denotes zero noise margin, and probable malfunctions of the device.

Figure 4.5 shows the minimum susceptibilities measured for line driver and receiver pairs. Line receivers were found significantly more susceptible than line drivers, so Figure 4.5 is actually a plot of susceptibility data measured for line receivers. As line receivers are the "weak link" of a line driver and receiver system, the susceptibility of the pair is adequately described by the susceptibility of the receivers alone. Line receivers were found to be approximately 7 dB more susceptible than line drivers. (However, line driver susceptibility lies within 0.5 dB of receiver susceptibility at 910 MHz). Figure 4.5 uses the receiver differential input voltage threshold (V_{th}) as the susceptibility criterion.

The strobe and response control terminals were found the most susceptible line receiver terminals. However, the strobe and response control terminals, unlike the inputs, are rarely connected to system interconnect lines, which may be the major receptors of RF energy. Thus, the susceptibility of the input terminals may be more important to the system designer than the susceptibilities of the other terminals. The inputs were found to be approximately 4 dB less susceptible than is indicated in Figure 4.5 (all points of which occurred with RF conducted into the strobe and response control terminals).

Threshold offsets have other effects on a signal besides reducing the noise margin. Where long lines are used, threshold offsets can cause time variations in

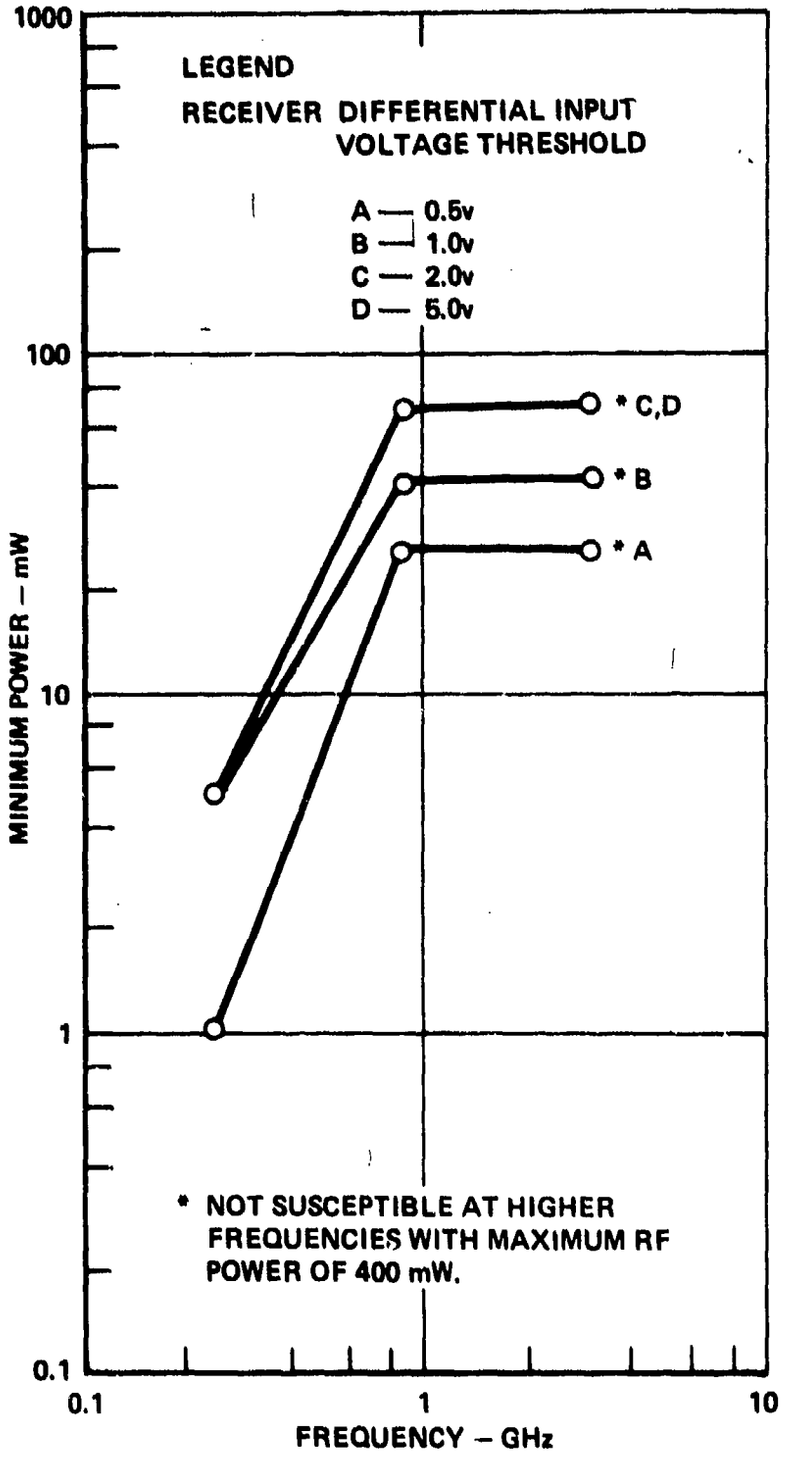


Figure 4.5. Worst Case Susceptibility Values for Line Drivers and Receivers

received signals from those sent by the driver. As a result, pulses may appear shifted in time in the received signal, or have longer or shorter durations than in the original signal. Reference 12 refers to the quality of a received signal in terms of "percent jitter". This is a ratio of the maximum relative time variations in the original and received signals to the minimum pulse period. For example, Figure 4.6 shows two pulse trains. The upper trace is the pulse train entering the driver, and which is to be sent by the system. The lower trace is the pulse train which emerges from the receiver after transmission via the long signal line (there would also be a propagation delay). In this example, the second pulse in the received train is shifted in time with respect to its position in the original train. The percent jitter is

$$\text{percent jitter} = \frac{\text{maximum variation in pulse position}}{\text{minimum pulse duration}} \times 100\%$$

$$= \frac{t_3 - t_2}{t_1} \times 100\%.$$

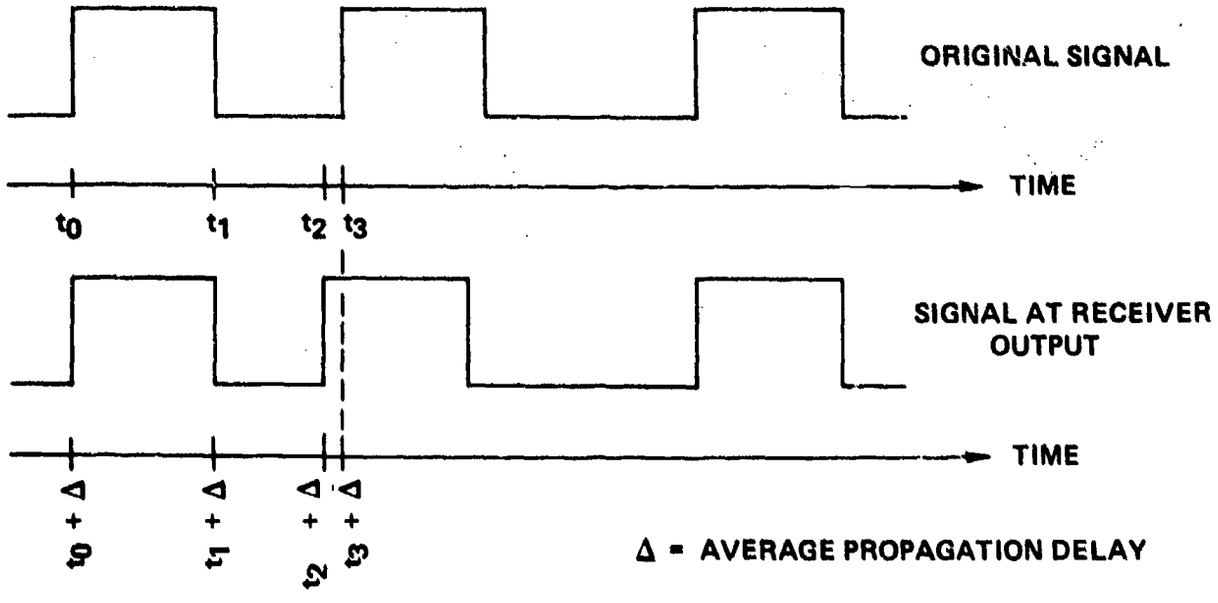


Figure 4.6. Illustration of Jitter in Signal After Transmission via Long Line

The jitter is related to the data rate (or minimum pulse width) and line length as shown in Figure 4.7. This graph was made using the following assumptions:

1) the driver 1 and 0 levels are matched exactly
2) the receiver threshold is exactly the mean of the 1 and 0 levels produced by the driver
3) time delays through both driver and receiver for both logic states are symmetrical and have zero skew
4) the line is perfectly terminated
5) the line charges at an exponential rate.

The line was assumed to have a time delay of 1.7 nsec/ft, which is a typical value for a twisted pair line. Reference 12 recommends that systems be operated with a minimum pulse width (t_{ui}) greater than 4 times the rise time of the line (t_r),

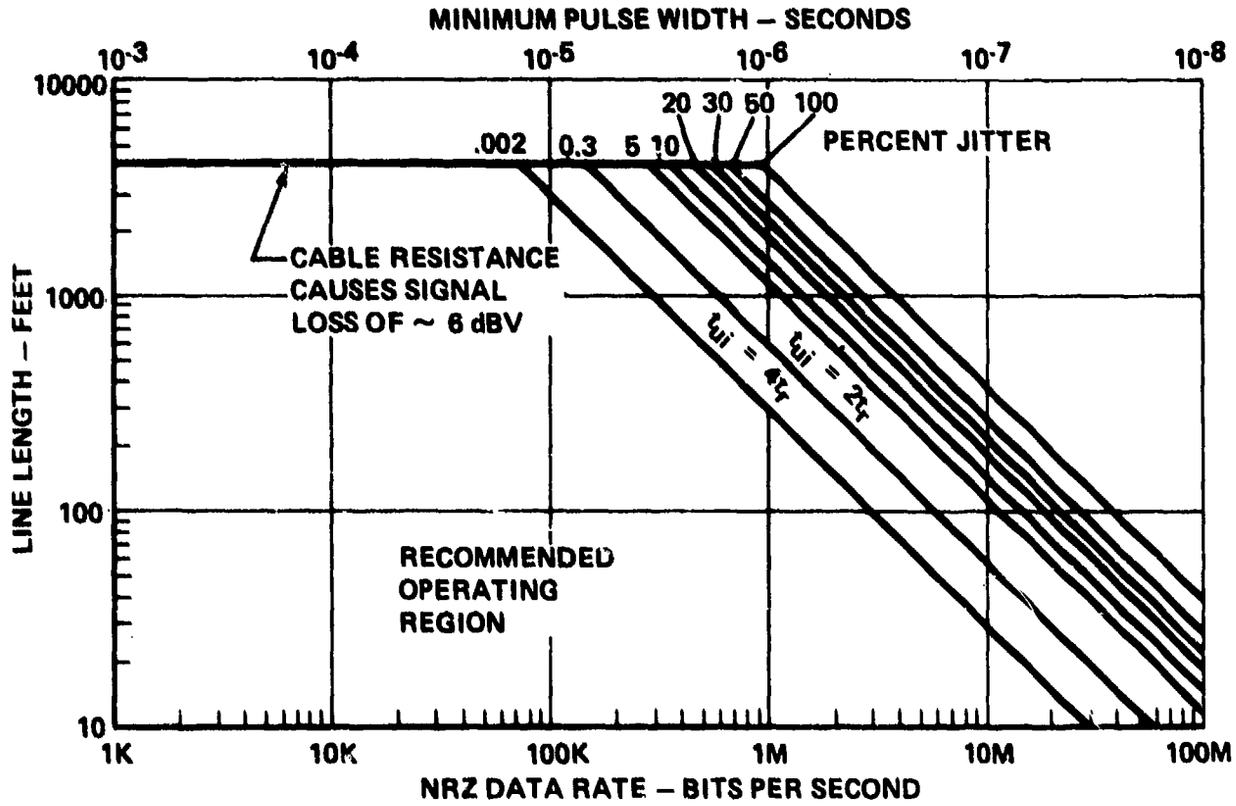


Figure 4.7. Signal Quality as a Function of Line Length and Data Rate

which gives a jitter less than 0.002% under these conditions. Data with jitter greater than 100% are probably not recoverable.

If the effects of threshold variations are included in Figure 4.7, the graphs shown in Figure 4.8 result. Here, the differential line voltage is assumed to be driven by voltages of $\pm V_{cc}$. Three conditions are shown: Figure 4.8(a) shows the jitter which results when the threshold voltage (V_{th}) is given by $-0.1\ V_{cc} \leq V_{th} \leq 0.1\ V_{cc}$, Figure 4.8(b) shows the jitter when $-0.2\ V_{cc} \leq V_{th} \leq 0.2\ V_{cc}$, and Figure 4.8(c) shows the jitter when $-0.4 \leq V_{th} \leq 0.4\ V_{cc}$. Figures 4.8(a) through (c) correspond to 0.5, 1.0, and 2.0 volt threshold changes for the receivers tested. Comparison with Figure 4.7 shows that the jitter increases due to threshold voltage variations.

As an example of the use of these graphs, suppose that a designer must drive a 100 foot line, and desires a jitter less than 5%. Figure 4.7 shows the maximum data rate to be 12 MHz. If the maximum interfering signal expected to enter the system is 1 mW at 220 MHz, Figure 4.5 shows that threshold variations of 0.5 volt may occur. Figure 4.8(a), which applies to the 0.5 volt threshold case, shows that a data rate of 12 MHz will result in approximately 15% jitter, substantially higher than the desired 5%. However, by reducing the data rate to 6 MHz, the 5% jitter requirement can be satisfied even with the interfering signal present. This example clearly illustrates that in high intensity electromagnetic environments it may be necessary to reduce the data transmission rate of a system.

4.5 Interference in Op Amps

Operational amplifiers are the most common type of linear integrated circuit, and are often used as functional blocks in more complex integrated circuits. The RF susceptibilities of several representative types of op amps were measured, and the results are presented in this section. Table 4.4 lists the types of op amps that were tested.

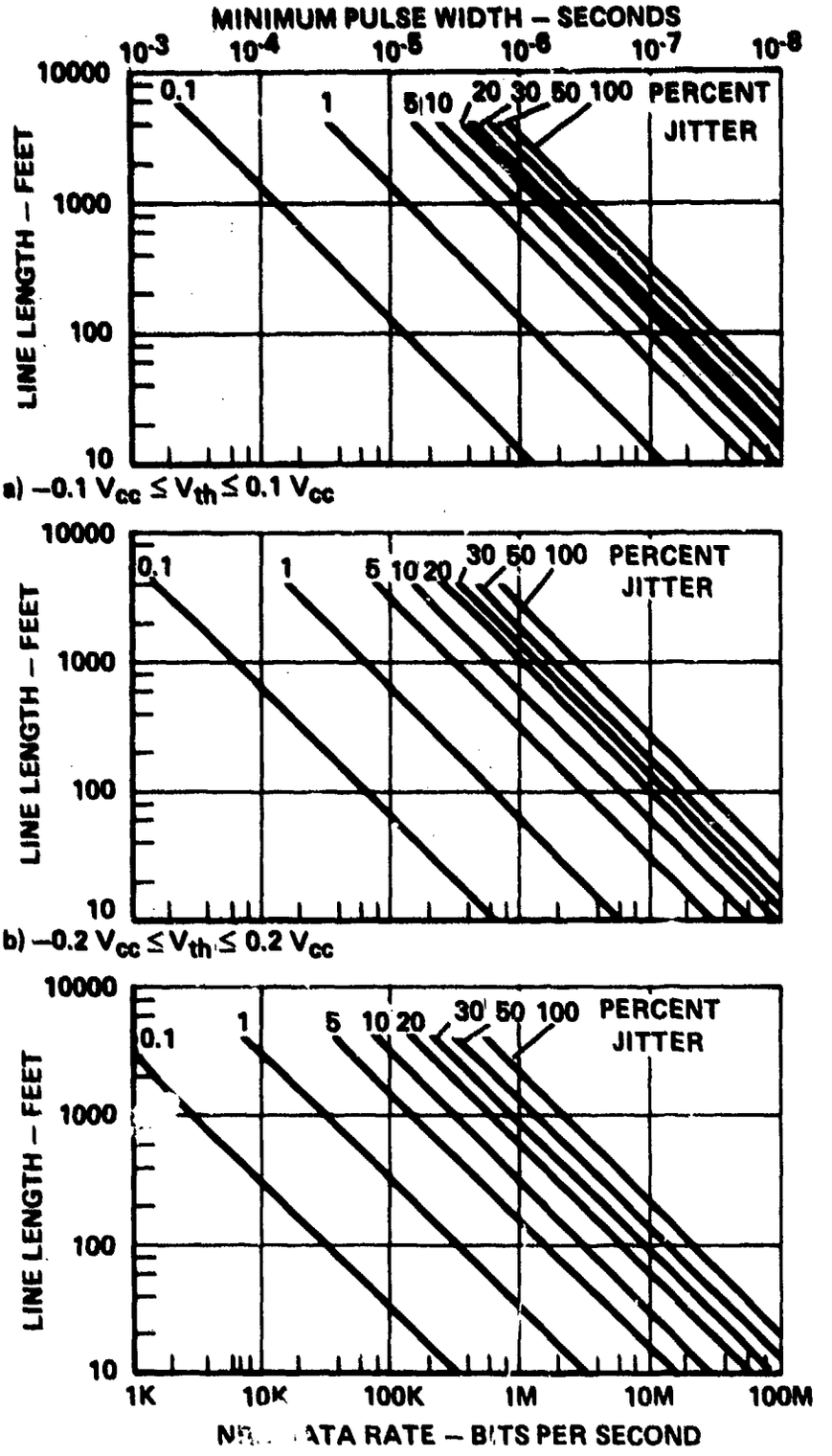
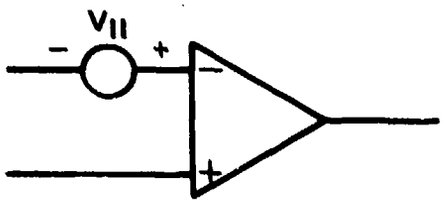


Figure 4. 8. Signal Quality as a Function of Line Length and Data Rate Including Effects of Threshold Voltage Offsets

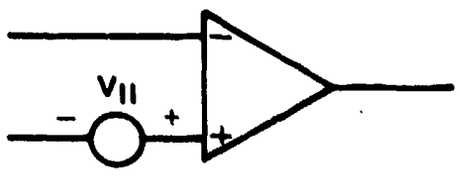
Table 4. 4. Op Amps Tested

741
108A
201A
207
0042C
531

Op amps were found most susceptible to RF energy conducted into either of the input terminals. When stimulated in this manner, the interference effect is an offset voltage at the particular input terminal entered by the RF. The magnitude of the offset voltage depends on such factors as the power level, frequency, equivalent RF source impedance, and the op amp input circuit. Figure 4.9(a) illustrates the offset voltage, represented by voltage generator V_{II}, which occurs due to rectification of an RF signal entering the inverting input terminal of the op amp. Figure 4.9(b) shows the location of the offset generator if RF enters the non-inverting input. If the op amp contains NPN input transistors, the polarity



a) RF ENTERS INVERTING INPUT



b) RF ENTERS NON-INVERTING INPUT

Figure 4. 9. Location of Offset Voltage Generator due to Rectification of RF Signal at Op Amp Inputs

of the offset generator is as shown, while if the input transistors are PNP type, the polarity of the offset generator will be reversed. More information on this simplified model of op amp interference is presented in Section 5.5.

The magnitude of the offset voltage generator v_{II} was used as the susceptibility criterion during the testing. Offsets of magnitude 0.05, 0.10, 0.15, and 0.20 volt were sought during the tests. Figure 4.10 shows the minimum RF power levels which were observed to cause offsets of these magnitudes. The required power levels are extremely small. At 220 MHz, only 1.2 μW is sufficient to cause an input offset voltage of 0.05 volt. Other effects were also observed during the testing, such as increases in the power supply currents, but these effects occurred at higher power levels than those at which significant input offset voltages occurred, or were linked to the input offset voltage through circuit interactions.

To illustrate the circuit interactions which occur when offsets appear at the op amp input terminals, Figure 4.11 shows an operational amplifier in a typical circuit: an inverting amplifier. If RF enters the inverting input, the offset generator v_{II} will appear as shown. Assuming first that the circuit is operating without interference ($v_{II} = 0$), the voltage v_{OUT} is given by

$$v_{OUT} = -v_{IN} \frac{R_F}{R_{IN}}, \tag{4.1}$$

i.e., the output voltage is directly proportional to the input voltage. If the effect of the offset generator is included, the output voltage becomes

$$v_{OUT} = -v_{IN} \frac{R_F}{R_{IN}} - v_{II} \left(\frac{R_F}{R_{IN}} + 1\right). \tag{4.2}$$

The interference effect seen at the output is a voltage offset proportional to v_{II}, and which depends on the values of the feedback resistors R_F and R_{IN}. The interference effect in other op amp circuits can be analyzed in a similar manner.

For offset voltages other than those shown in Figure 4.10, the minimum

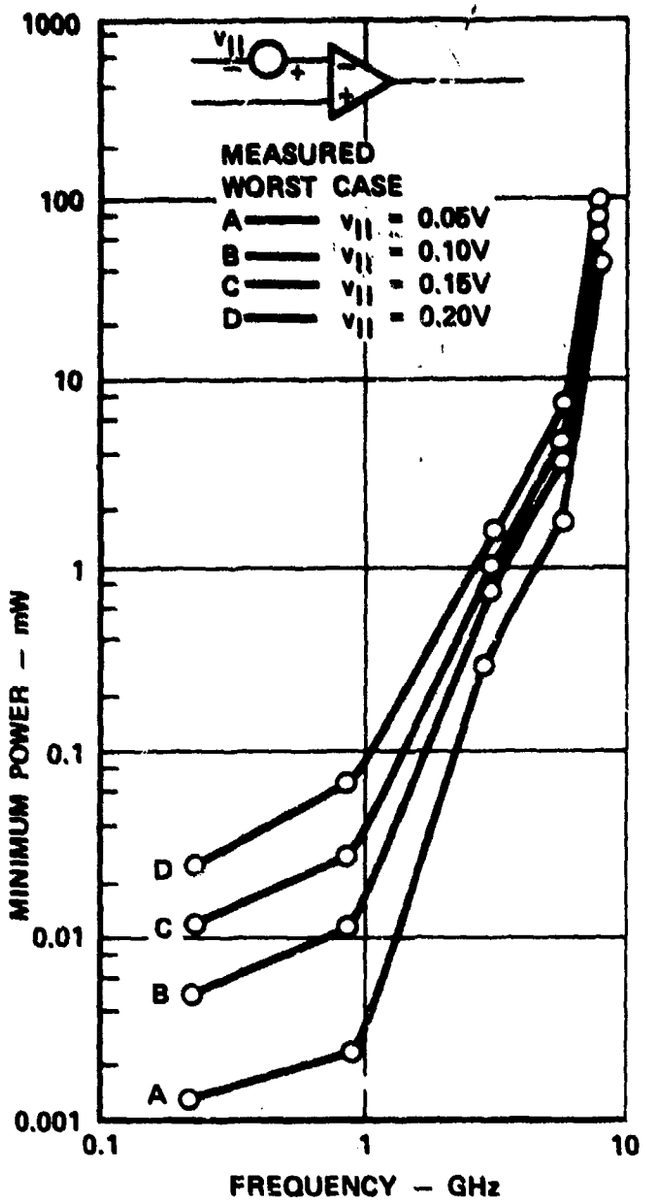


Figure 4.10. Worst Case Susceptibility Values for Op Amps

susceptibility levels can be estimated from the data of Figure 4.10. For offsets of magnitudes less than 0.05 volt, the offset voltage is approximately proportional to the minimum RF power level, $P(f, v_{II})$. ($P(f, v_{II})$ indicates that the minimum power level is a function of frequency and offset voltage). For offsets greater than 0.20 volt, the offset voltage is approximately proportional to the square root of the RF power level. Thus, to estimate the minimum powers to cause offsets not

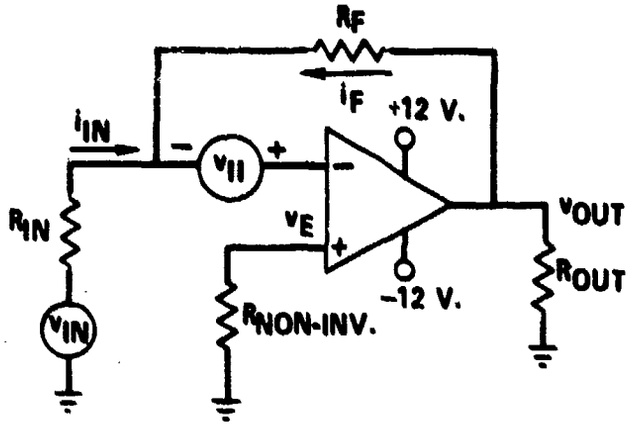


Figure 4.11. Inverting Amplifier Circuit with Offset Generator Shown at Op Amp Inverting Input Terminal

shown in Figure 4.10, a reasonable procedure is

$$P(f, v_{II}) = \begin{cases} \left(\frac{v_{II}}{0.05V}\right) \cdot P(f, 0.05V) & \text{for } v_{II} < 0.05V \\ \text{use figure 4.10} & \text{for } 0.05V \leq v_{II} \leq 0.20V \\ \left(\frac{v_{II}}{0.20V}\right)^2 \cdot P(f, 0.20V) & \text{for } v_{II} > 0.20V, \end{cases} \quad (4.3)$$

where P(f, 0.05V) and P(f, 0.20V) are determined from Figure 4.10 at the desired frequency.

4.6 Interference in Voltage Regulators

Voltage regulators are common linear integrated circuits, of which many types are available. Most voltage regulators can be grouped into two general categories: 3-pin regulators and multi-pin regulators. The 3-pin regulators have (as their name implies) only 3 terminals: input, output, and ground. They have fixed output voltages which are available in several common voltage values. Three-pin regulators enjoy widespread use because they require no external components.

Multi-pin regulators have additional terminals which make them more versatile than 3-pin regulators. They can, for example, supply a variable output voltage, or be used in shunt, switching or floating operation, etc. Generally, they have 4, 8, or 10 terminals. In use, they require external components, usually resistive

dividers and compensation capacitors, but their versatility makes them attractive for use in many designs.

Measurements were made of the RF susceptibility of both 3-pin and multi-pin regulators. Testing was done on 3-pin regulators having a nominal output voltage of 5 volts, and on multi-pin regulators with 8 pins. Table 4.5 lists the types tested.

Table 4.5. Voltage Regulators Tested

3-PIN (5 VOLT)
309
320
78M05
8-PIN
300
305

The 3-pin regulators were tested with a 7 volt input voltage and six different load conditions: output currents of 1 mA, 20 mA, 50 mA, 100 mA, 150 mA and 200 mA. The susceptibility criterion was an output voltage below 4.75 volts or above 5.25 volts. RF was conducted into each of the three pins individually; RF entering the output was found to be the most susceptible case. At 220 MHz, devices were found susceptible to 1.3 mW minimum power. The susceptibility levels increase at higher frequencies. A plot of the susceptibilities of 3-pin regulators is shown in Figure 4.12.

The 8-pin regulators were tested in the configuration shown in Figure 4.13. The input voltage was 18 volts, and the output voltage divider was chosen to yield a nominal 12 volts output voltage. As the actual output voltage varied somewhat for different types due to manufacturing variations, the susceptibility

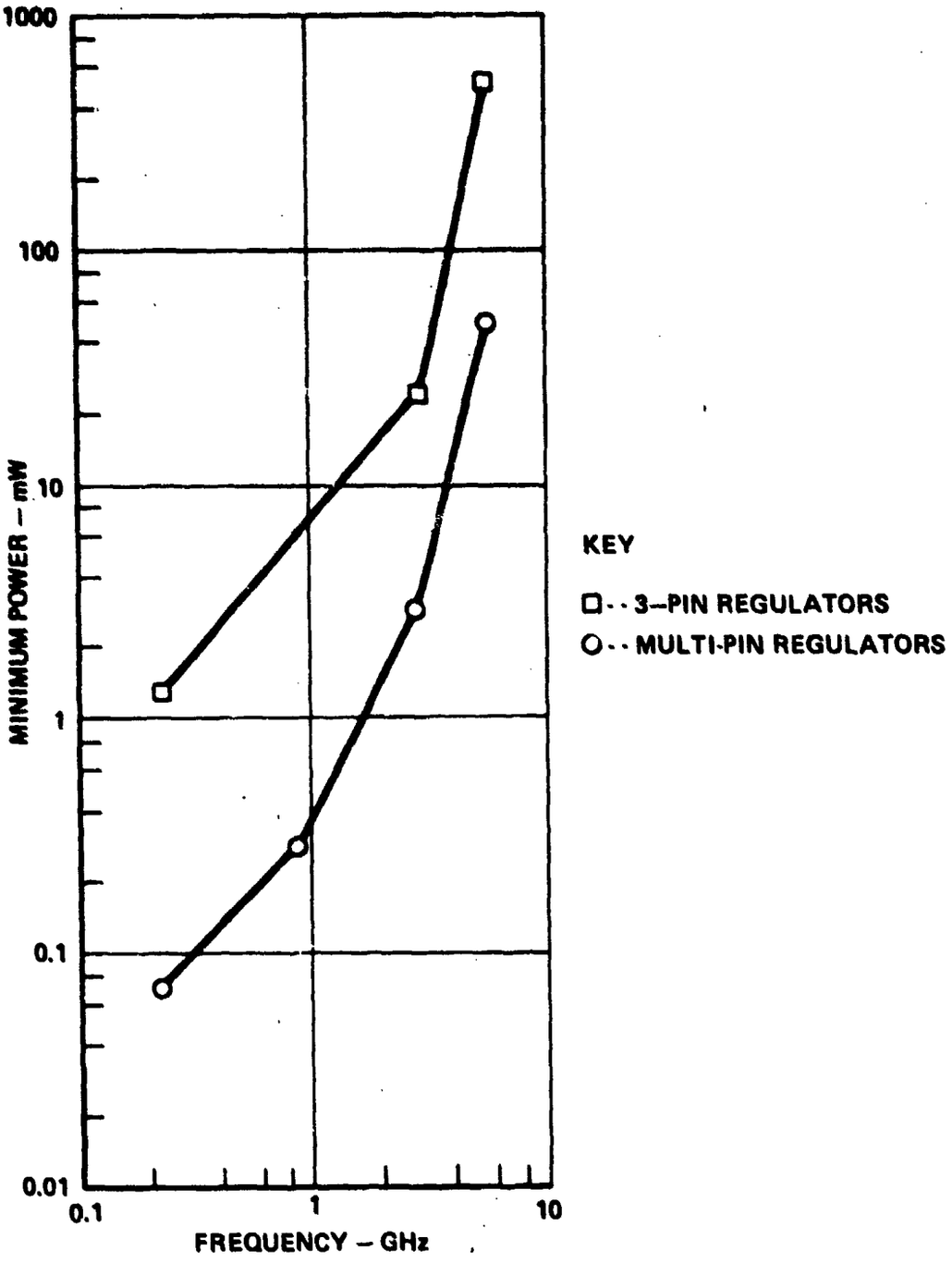


Figure 4. 12. Worst Case Susceptibility Values for Voltage Regulators. Output Voltage Change of 0.25 Volt is Susceptibility Criterion.

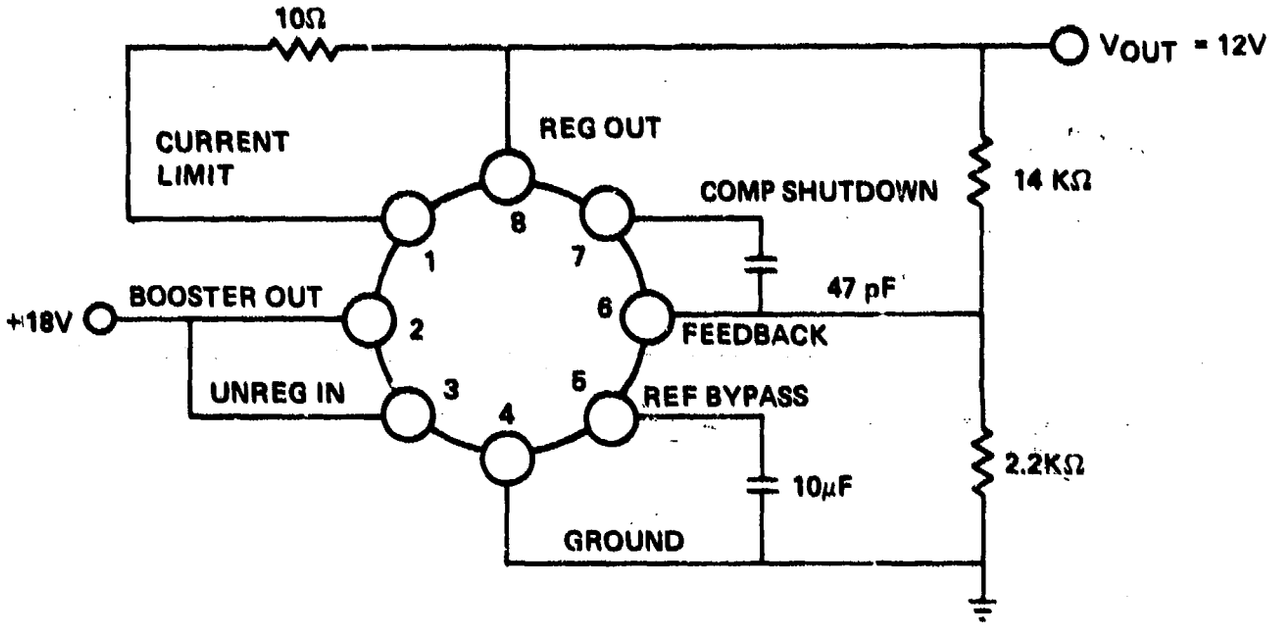


Figure 4. 13. Circuit for 8 Pin Voltage Regulator Susceptibility Tests

criterion was a 0.25 volt change in the output voltage from the no RF case for that device. Figure 4.12 shows the minimum susceptibilities for the 8-pin devices. The most susceptible cases occurred for RF conducted into the reference bypass and feedback terminals.

Examination of Figure 4.12 indicates that the 8-pin voltage regulators are quite susceptible. At 220 MHz, only 0.07 mW of RF power is required to cause interference. The susceptibility values approach those of op amps, which have been shown to be sensitive to RF powers as low as 1 μW. Analysis of the regulator circuit reveals why this is so. Figure 4.14 is a functional diagram of the basic regulator circuit. In multi-pin regulators, the op amp, series pass element, and voltage reference are internal to the chip, while the voltage divider consisting of R_1 and R_2 is external. A feedback circuit is formed that drives the voltage across resistor R_2 to the value of the reference voltage. The output voltage is then determined by the values of resistors R_1 and R_2. The presence of the op amp, however, causes the device susceptibility to be quite high. When RF is conducted

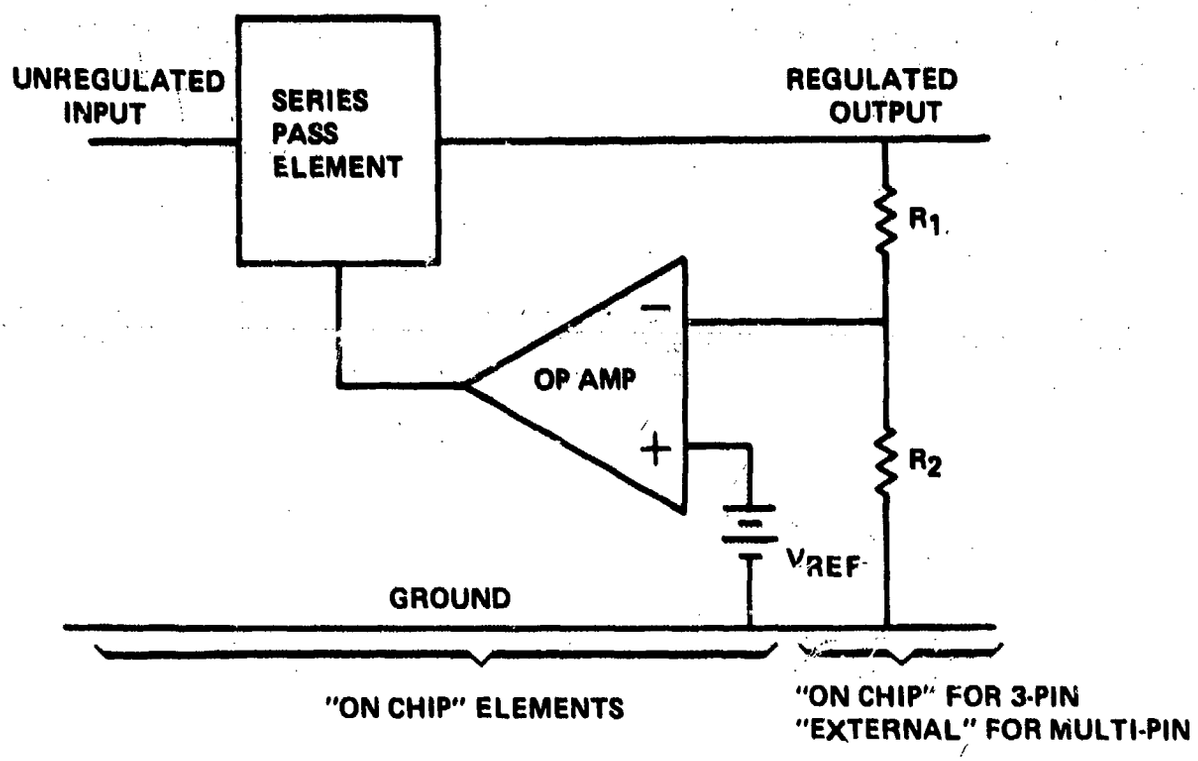


Figure 4. 14. Basic Series Regulator Circuit

into the pins corresponding to the op amp inputs, the signal is rectified, and an offset voltage appears at the amplifier input terminals. The offset voltage upsets the op amp's ability to compare the voltage across R_2 to the reference voltage, resulting in a deviation in the output voltage.

In 3-pin regulators, the resistive divider is built directly on the chip, so the amplifier inputs are inaccessible at the regulator terminals. Hence, RF cannot directly enter the op amp inputs, and the device susceptibility is much lower. As shown in Figure 4.12, 3-pin regulators are about 12 dB less susceptible than multi-pin regulators. The difference in susceptibilities of the two types may be significant to designers and EMC engineers.

In the 8-pin regulator testing, the compensation and bypass capacitors were located outside the RF test fixture, so that they had no effect on the incoming RF energy. However, in an actual application, these capacitors may offer a degree of protection by shunting the RF energy away from the amplifier inputs.

The offset voltage observed at the amplifier inputs in multi-pin regulators can be modeled in the same manner as the input offset voltage for op amps. The simplified model shown in Figure 4.9 adequately accounts for the offset voltage at the reference amplifier terminals.

4.7 Interference in Comparators

Comparators are common linear integrated circuits used to detect voltage levels in electronic equipment. Measurements were made of the RF susceptibility of several types of comparators. Table 4.6 lists the types tested.

Susceptibility was defined in terms of changes in the input-output voltage transfer curve of the comparator. Figure 4.15 illustrates a typical transfer curve for a 710 type comparator. The output switches between high and low values at an input voltage between -1.0 mV and +1.0 mV. Manufacturer specifications guarantee that this switching will occur at input voltages between -3.0 mV and +3.0 mV.

RF energy conducted into the comparator can cause the transfer curve to change and, in particular, the comparator switchpoint changes. An offset in the comparator switchpoint has an adverse effect on the comparator's accuracy when used to detect voltage levels in circuits. Switchpoint offsets of $\pm$0.05, $\pm$0.10, $\pm$0.20, and $\pm$0.50 volt, representing varying degrees of interference effect, were sought in the testing. Figure 4.16 illustrates the minimum powers observed to cause interference as defined by these four susceptibility criteria. The devices were susceptible to a minimum of 0.025 mW at 220 MHz using the 0.05 volt offset criterion as the definition of susceptibility.

The testing revealed that comparators are the most susceptible to RF energy conducted into the input terminals. This is expected, since comparators contain a differential pair input stage similar to that contained in op amps, which are very sensitive to RF conducted into their input terminals. Rectification of the RF

Table 4. 6. Comparators Tested

306

311

339

360

710

760

signal causes an offset voltage to appear at the input terminal into which the RF is conducted, which causes a similar offset to occur in the comparator switchpoint. This effect could be modeled by placing an offset voltage generator in series with the input terminal that the RF is entering, as shown for op amps in Figure 4.9. The polarity of the offset generator depends on the input circuit that rectifies the RF signal. For example, if the input transistors of the differential pair are

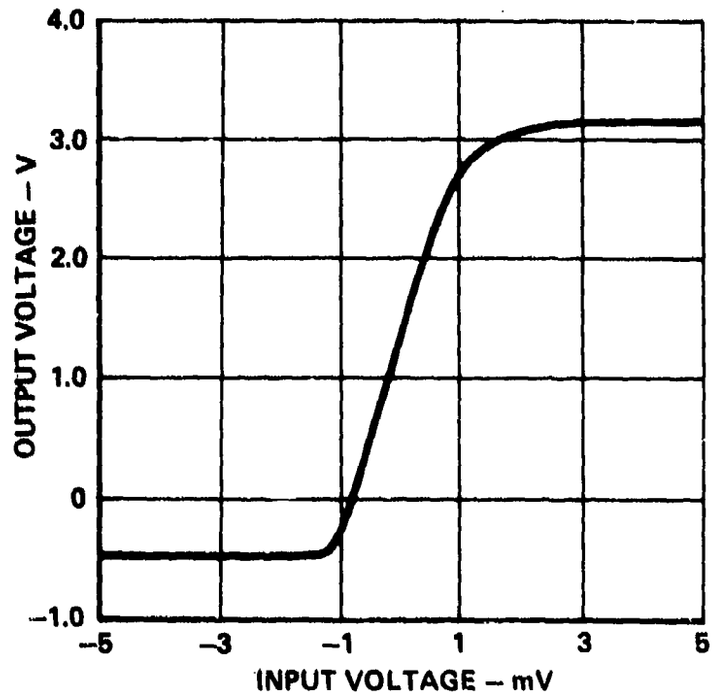


Figure 4. 15. Typical Voltage Transfer Curve for Type 710 Comparator

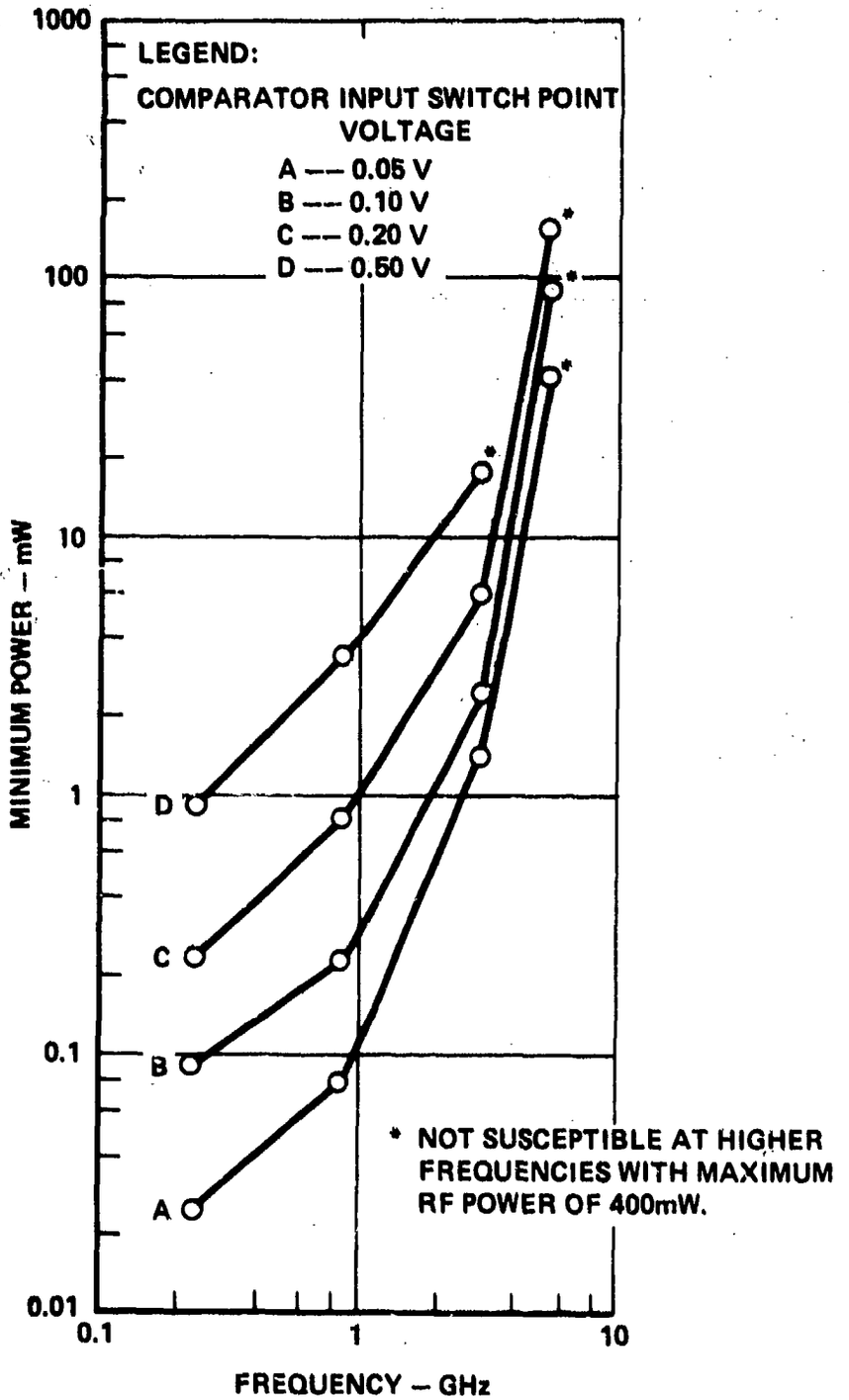


Figure 4. 16. Worst Case Susceptibility Values for Comparators

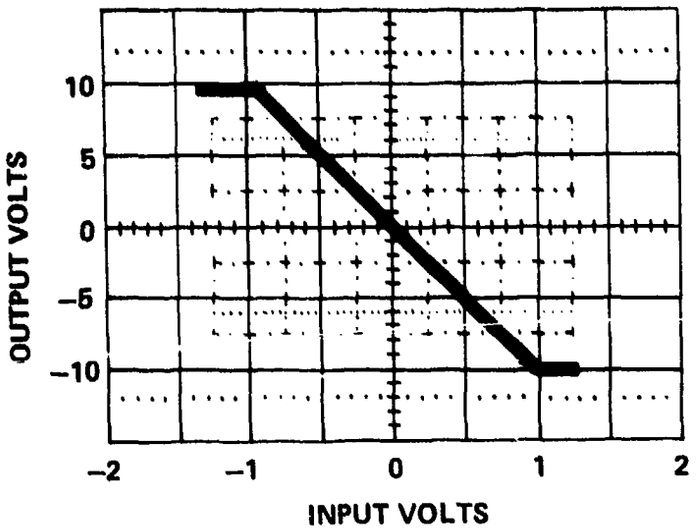
NPN types, the polarity of the offset generator is as shown in Figure 4.9(a): the positive terminal of the offset generator lies at the comparator input. If the input transistors are PNP type (as in 311 type comparators), the offset generator has the opposite polarity. The magnitude of the offset depends on the RF power level, frequency, and equivalent RF source impedance.

4.8 Burnout in Integrated Circuits

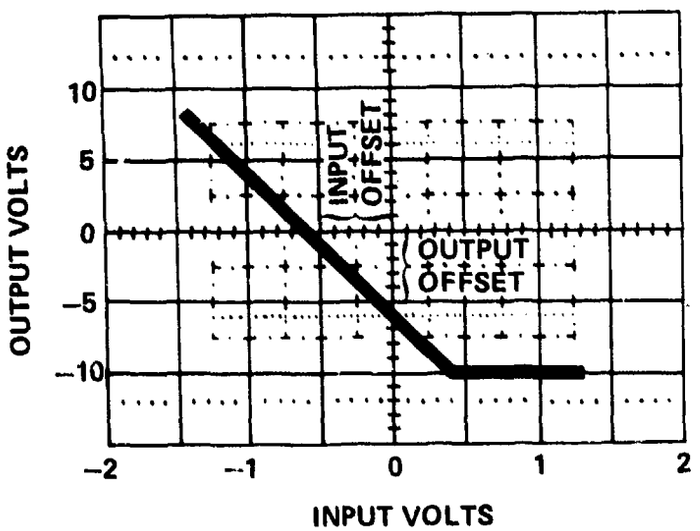
Integrated circuits can suffer permanent damage from sufficiently intense microwave signals. The energy in an RF signal can be sufficient to cause thermal failures in the silicon junctions, the metallization stripes, or the bond wires. The significance of the damage suffered by the IC is determined by its ability to function after injection of the RF signal. If the device can still function in a limited capacity after the RF stimulus is removed, the device is considered degraded. For example, Figure 4.17(a) shows the transfer curve of an amplifier circuit containing an operational amplifier. The circuit is an inverting amplifier with a gain of 10. After exposing the op amp input circuit to a high level pulsed RF signal, the transfer curve changes as shown in Figure 4.17(b). Large offset voltages result in the amplifier characteristics. This degradation occurs when one of the input transistors in the op amp suffers a thermal junction failure.

The difference between degradation and catastrophic failure is in the criticality of the part damaged. Catastrophic failure is defined as complete inability of the device to perform its intended function. The criticality of the damage is more dependent on the location of the damage rather than on the type of damage mechanism. For instance, while a metallization failure may only cause degradation if it occurs in the offset null circuit of an op amp, a similar metallization failure in the output circuit will cause catastrophic failure.

This section provides information on the minimum energy sufficient to cause permanent damage to occur in integrated circuits, regardless of whether degradation



a) Transfer Curve for Amplifier Circuit Containing 741 OP AMP



b) Transfer Curve for Amplifier Circuit Containing Degraded 741 OP AMP

Figure 4.17. Effect of Degraded OP AMP on Amplifier Circuit (V_S = ± 12 Volts)

or catastrophic failure occurs. Results of both laboratory tests and analysis using thermal models are presented to define the power levels at which burnout is expected to occur in integrated circuits.

During the laboratory testing over 2500 devices were exposed to microwave signals varying in frequency, pulse width, and power level. After exposure, the failed devices were opened and examined under a microscope to determine the exact

mechanism of failure. Three types of mechanisms were observed, all thermal in nature: bond wire failure, junction failure, and metallization failure. Figures 4.18, 4.19, and 4.20 are photographs showing typical examples of a bond wire, a junction, and a metallization failure, respectively. These types have been observed to occur both singly and in combination throughout the high power RF testing. Figure 4.21 illustrates the pulse power levels observed to cause failure in integrated circuits versus the pulse width. The upper shaded region locates those pulse powers and pulse widths at which failures have been observed. No failures have been observed at RF power levels below 0.5 watt.

Since the damage mechanisms are thermal in nature the damage models are derived from basic heat flow analysis. For worst case analysis the heat is assumed to be produced by I^2R dissipation of the RF signal and there is no frequency dependence. RF power level and pulse duration are the important parameters.

The bond wire model assumes the wire is a rod with a perfect heat sink at each end and the RF power is dissipated uniformly through the wire volume. Since the temperature is highest in the center of the wire, the desired solution of the heat flow problem is a power versus time relationship to raise the temperature at the center of the wire to the melting point. The latent heat of fusion actually required to melt the wire is assumed negligible so that the solution gives a theoretical relationship:

$$P = \frac{8\,AK(T_f - T_o)}{L\left[1 - \frac{32}{\pi^3} \sum_{n=1,3,5\ldots}^{\infty} \left(\frac{1}{n^3}\right)\left(\exp\left(\frac{-n^2\pi^2 kt}{L^2}\right)\right)\left(\sin\frac{n\pi}{2}\right)\right]} \qquad (4.4)$$

where P is power in watts,

t is time in seconds,

k is thermal diffusivity of wire material in cm^2/sec,

K is thermal conductivity of wire material in watts/cm/°C,

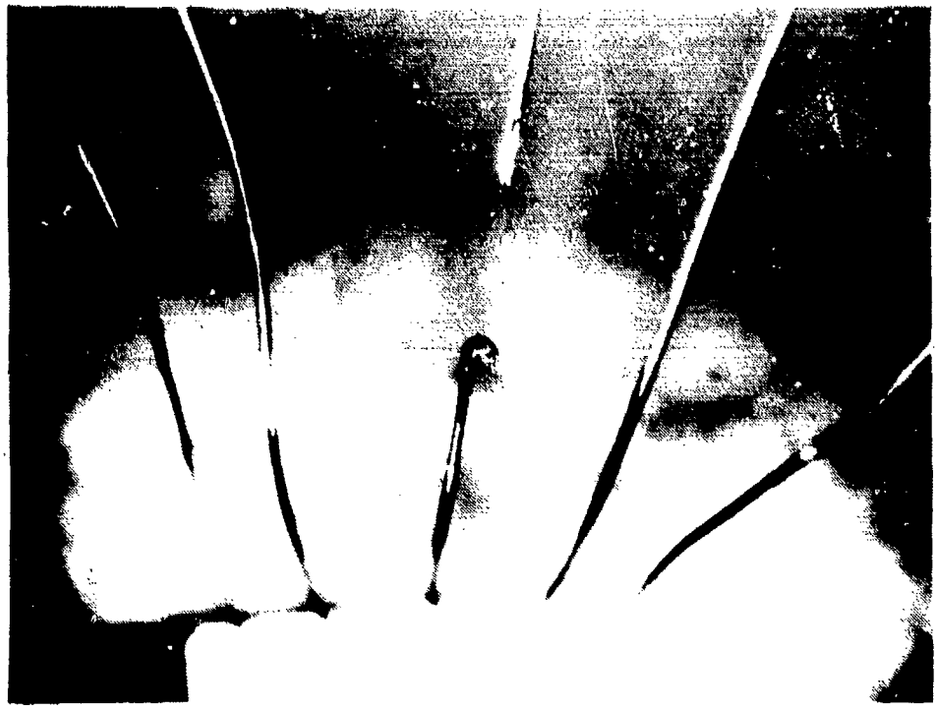


Figure 4.18. Photograph of Bond Wire Failure

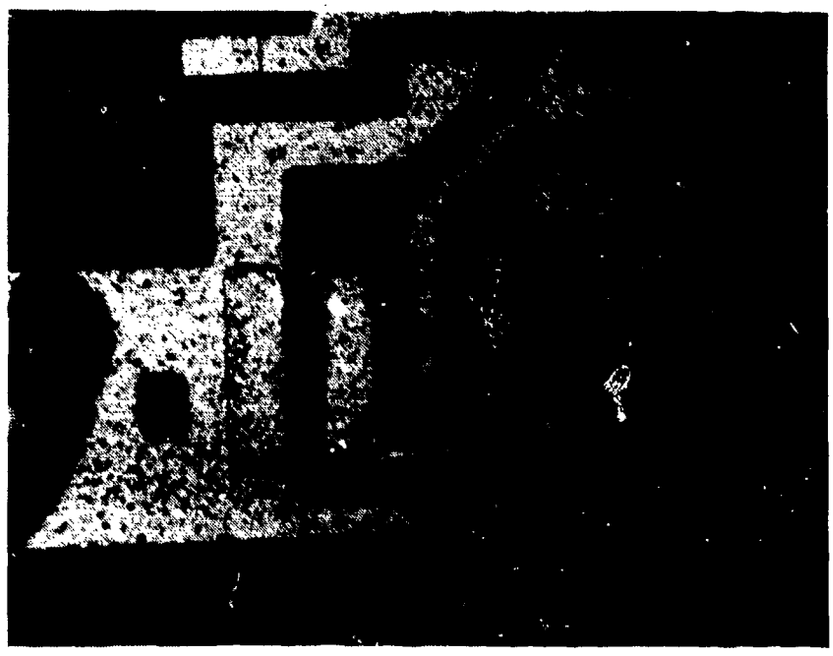


Figure 4. 19. Photograph of Collector-Emitter Junction Failure in the Output Transistor of a 7400 NAND Gate

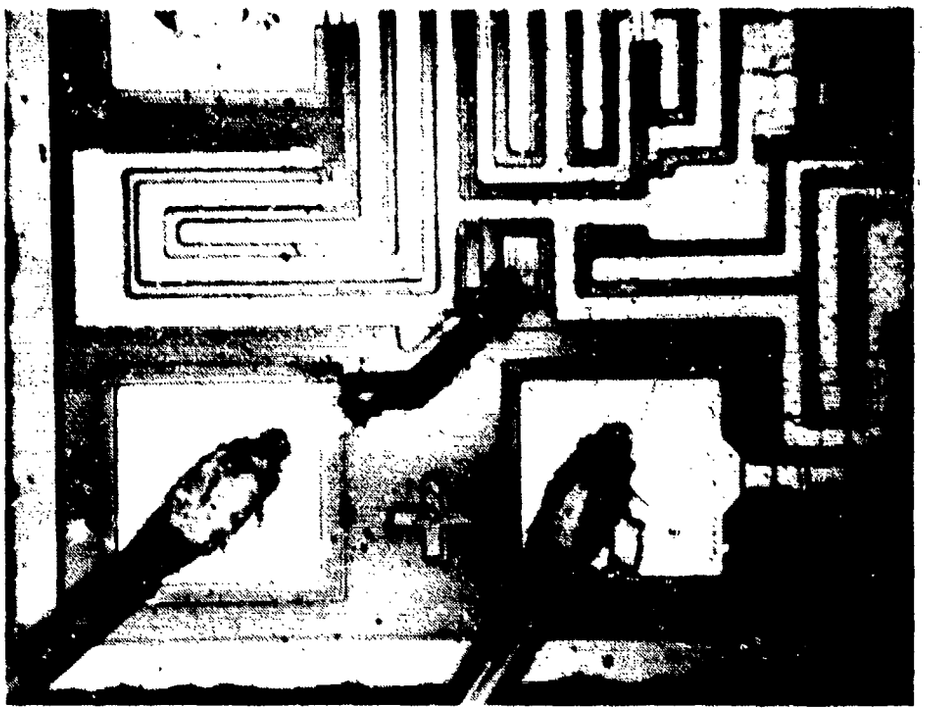
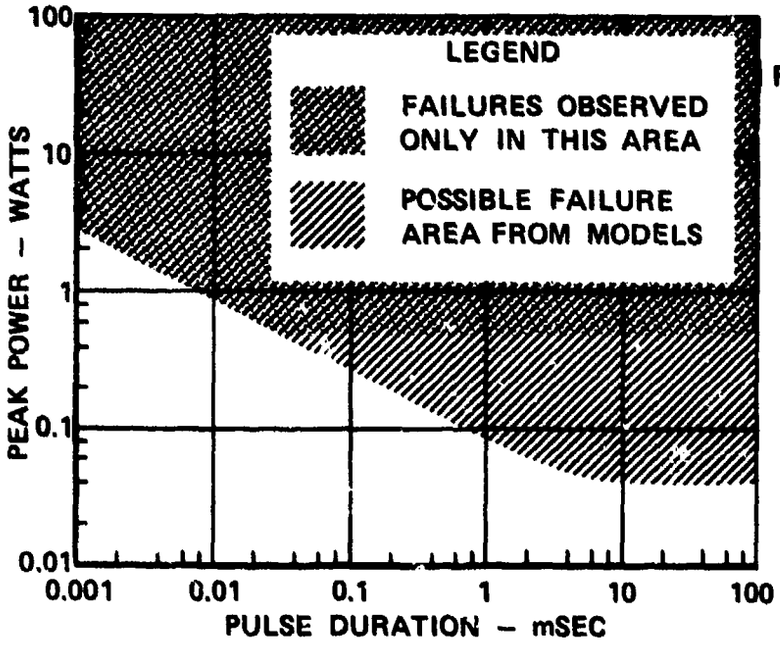


Figure 4.20. Photograph of Metallization Failure in the Input Lead of a CMOS 4011 NAND Gate



FAILURE MODELS FOR:
BOND WIRE
ALUMINUM
DIAMETER $\geq$ 0.001778 cm
LENGTH $\leq$ 0.5 cm
JUNCTION
SILICON
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS $\leq$ 0.032 cm
METALLIZATION
ALUMINUM
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS $\leq$ 0.032 cm

Figure 4.21. Measured and Predicted Worst Case Failure Levels

A is wire cross-sectional area in cm^2,

L is wire length in cm,

T_f is wire melting temperature in °C,

and T_o is ambient temperature in °C.

The failure models for the junction and metallization damage modes are essentially identical. In both cases, the source of heat can be described as a thin sheet (of either silicon or aluminum) where it is assumed that all the power is being dissipated. Since the sheet is very thin, it is assumed that a uniform temperature exists through the thickness of the sheet and both cases can be treated as uniform surface heating. Both models reduce to the same boundary value problem where heat is conducted away from one surface through the silicon chip. The junction and metallization failure models assume one dimensional heat flow through the silicon chip. The lower surface of the chip is assumed to be attached to a perfect heat sink which remains at ambient temperature. The silicon chip initially is at ambient temperature. The power to produce failure temperature T_f in time t is given by:

$$P = \frac{\left(\frac{T_f - T_o}{L}\right) KWD}{1 - \frac{8}{\pi^2} \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n^2} \left(\exp\left(-kn^2\pi^2 t/4L^2\right)\right)\left(\sin\frac{n\pi}{2}\right)} \qquad (4.5)$$

where the area of the failure site (metallization stripe or junction) is given by the product of W (width in cm) and D (length in cm) and L is the thickness of the silicon chip in cm.

The worst case assumption used for the failure models is that all the incident power is actually absorbed in the failure site. This assumption is conservative since it does not account for the power dissipated elsewhere in the chip. Also worst case values are used for the physical parameters in the predictions to calculate the minimum power to cause failure. For example, the minimum bond wire diameter in current use is 0.001778 cm (0.7 mil) and a length of 0.5 cm is as long

as can be reasonably expected. For junction or metallization failures, the area of the junction or stripe is the primary factor affecting a worst case prediction of failure. The worst case areas for junction and metallization failures are both assumed to be 6×10^{-6} cm^2 (a representative failure site area based on actual measurements). The worst case failure temperature for the junction model was taken to be 660°C (anything hotter would presumably melt the aluminum metallization first).

Figure 4.21 illustrates the failure levels predicted by the worst case thermal modeling. The shaded regions show the pulse powers at which damage may occur according to this analysis. The power levels at which failure are predicted are approximately 11 dB below those at which failures have actually been observed. This difference is due to the conservative assumptions made in the analysis, including the physical dimensions and the assumption that all of the incident power is absorbed at the failure site. Because of these worst case assumptions, it is fairly certain that failures will not occur outside the shaded regions of Figure 4.21.

When considering pulse trains, two conditions must be met to preclude burnout. The first condition is concerned with the peak power and pulse width of individual pulses in the train. To prevent burnout due to a single pulse, the peak power versus pulse width for each pulse must lie outside of the shaded region of Figure 4.21. The second condition is that the average power of the pulse train should not exceed the power sufficient to cause failure from a single pulse of the same length as the pulse train. For very long pulse trains, the following condition must be satisfied:

$$P_{peak} \cdot PW \cdot PRF \leq P_{cw} \tag{4.6}$$

where P_{peak} is the peak pulse power,

PW is the pulse width,

PRF is the pulse repetition frequency, and

P_{CW} is the power sufficient to cause failure from a CW signal. From Figure 4.21 we see that theoretically P_{CW} can be as low as 40 mW, but a more realistic value for P_{CW} based on observed failure levels is 500 mW. (The product PW · PRF is commonly called the duty cycle). Burnout is possible if either of these two conditions is not met.

From Equation (4.6) and using P_{CW} = 500 mW, we find that if PRF < 33 KHz, a single pulse will produce failure (whenever a failure actually occurs), so that Figure 4.21 can be used. When PRF > 33 KHz, failure can occur from either a single pulse or the average power of the pulse train, so that both conditions given above must be considered in determining whether burnout can occur.

CHAPTER 5

INTERFERENCE MODELING

As described in Chapter 4, susceptibility measurements were made on a large number of integrated circuits. The measurement program yielded a good estimate of the susceptibilities of these circuits under well-controlled laboratory conditions although worst case conditions were estimated for conservatism. The objective of modeling is to gain a greater understanding of the phenomena involved to increase confidence in the extrapolation of the measured data, and to extend the results to devices and configurations not actually tested.

The observed interference effects are attributable to rectification of the RF or microwave signal in the PN junctions of the integrated circuit. Essentially, the signal is envelope detected by the nonlinear characteristics of the semiconductor junctions. In a typical integrated circuit, which may contain over 20 transistors and diodes as well as a multitude of parasitic PN junctions, the modeling problem becomes quite formidable.

This chapter briefly outlines the approach taken to model interference effects in integrated circuits. Section 5.1 describes a circuit model developed to account for large-signal rectification in individual PN junctions, and the results of parametric studies to determine the expected range of each of the model parameters. Section 5.2 describes a model for interference in transistors, which is based on modifications to the standard Ebers-Moll representation, and uses the junction interference model of Section 5.1 as an integral element. Section 5.3 describes the use of these models in analyzing the interference effect in a TTL NAND gate, using the computer-aided circuit analysis program SPICE, while Section 5.4 continues the example by describing a worst case analysis procedure on the circuit. Section 5.5 is an example of modeling interference in op amps, using macromodeling techniques and the timesharing circuit analysis program ISPICE.

5.1 Rectification in PN Junctions

Rectification is the mechanism through which out-of-band RF or microwave signals are converted to in-band signals. The process is essentially envelope detection. Unwanted signals are unintentionally detected by devices intended to perform other functions. The detected response varies with the envelope of the RF signal, which depends on the characteristics of the RF source. For example, a pulsed radar may stimulate interference in the form of video pulses in electronic equipment, while certain communications transmitters will cause nearly constant offset voltages and currents to occur. These signals may be indistinguishable from those normally present in the circuit. In fact, once an RF signal is rectified and alters a data stream or analog level, it is difficult, if not impossible, to remove the interference effect with additional processing. At this time, the best assurance that interference will not occur in a circuit is to reduce the RF to safe levels through adequate shielding.

Rectification occurs because of nonlinearities inherent in semiconductor devices. All semiconductors are built of PN junctions which have a nonlinear current-voltage characteristic. In general, a PN junction experiences a decrease in dc voltage and an increase in dc current when stimulated with a continuous RF signal. Figure 5.1 illustrates a piecewise linear video model of a PN junction which includes rectification effects. It contains two diodes, a current source, and a resistor. Diode D1 models the diode with no RF stimulation, and obeys the standard diode equation:

$$i_{D1} = I_{DS}\left(e^{\frac{qv_D}{kT}} - 1\right), \tag{5.1}$$

where: i_{D1} is the current through diode D1,

v_D is the voltage across D1,

I_{DS} is the diode reverse saturation current,

q is the electron charge,

k is Boltzmann's constant, and

T is the junction temperature in degrees Kelvin.

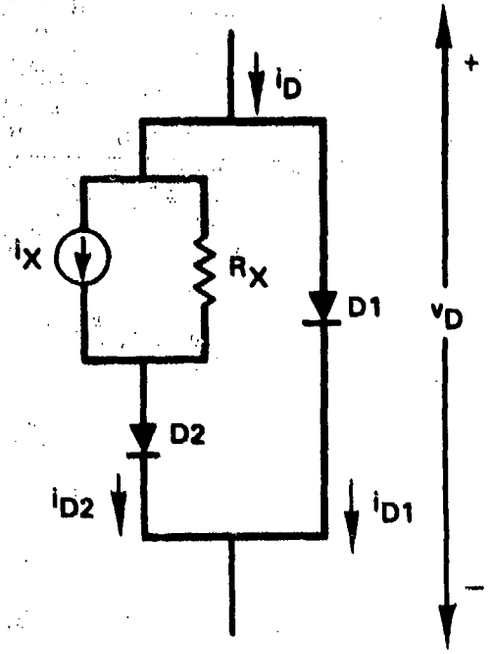


Figure 5.1. Circuit Model of Diode under RF Influence

The Norton equivalent comprised of i_X and R_X, and diode D2 model the video current and voltage offsets due to RF. For simplicity, diode D2 is assumed to have the same characteristics as D1. The value of current source i_X depends on the RF power level, frequency, and RF source impedance. For large RF signals (i.e., RF voltage comparable to, or greater than kT/q), i_X is proportional to the square root of the RF power level. Thus,

$$i_X = K\sqrt{P_{RF}}, \tag{5.2}$$

where K is a constant dependent on the frequency and source impedance of the interfering RF signal. The value of R_X also depends on the frequency and source impedance of the RF signal, but is independent of power level. In general, R_X increases with increasing frequency or increasing source impedance, while K decreases.

For modulated RF signals, the value of current source i_X varies with the envelope of the signal. The RF power level, P_{RF}, follows the instantaneous envelope of the RF signal, and the instantaneous value of i_X is given by Equation (5.2).

An analysis involving ideal diodes yields an estimate of the expected ranges of the parameters K and R_X. The RF source (which models the pickup mechanism described in Chapter 3) is represented by a Thevenin equivalent consisting of a voltage source $V_S \sin \omega t$ in series with an impedance $R_S + jX_S$, which represents the RF impedance of the source as seen from the diode. The diode junction is modeled by an ideal diode with a constant shunt capacitance C and series resistance, r_S. Through a time domain analysis of junction waveforms, the RF induced rectification by the diode can be deduced, and the corresponding PN junction model parameters found. Referring to Figure 5.1, the value of R_X is

$$R_X = ((R_S + r_S)^2 + X_S^2)^{1/2} ((1 + \omega C X_S)^2 + (\omega C)^2 (R_S + r_S)^2)^{-1/2}, \qquad (5.3)$$

and the value of K is

$$K = (8R_S)^{1/2} ((R_S + r_S)^2 + X_S^2)^{-1/2}, \qquad (5.4)$$

where the incident RF power, P_{RF}, is related to V_S and R_S by

$$P_{RF} = V_S^2/8R_S. \qquad (5.5)$$

Equation (5.5) represents a constraint on the possible values of V_S and R_S which is imposed by the ability of realizable power sources to deliver power to a conjugate load. There are no apparent constraints on the value of X_S, and, in general, one must consider that any value is possible. The term r_S can be considered to represent lossy factors in general, whether associated with the junction itself (e.g. bulk resistance) or the lossy transmission lines inevitably encountered in real world interference problems.

Computer-aided studies of the effects of the parameters R_S, r_S, and X_S on the video model parameters K and R_X together with analysis of max-min conditions show that the values of K and R_X (which always occur as ordered pairs) occupy a definite region in the K-R_X plane. For the absolute worst case of no extrinsic loss (i.e., $r_S=0$), the region of the K_X-R_X plane in which possible values of K and R_X lie is shown in Figure 5.2. The upper boundary is described by the relation

$$K_{max} = (8/R_X)^{1/2} \qquad (5.6)$$

The lossy element r_S provides a degrading effect on the rectification, and limits the maximum value of K which can occur. For a given value of r_S, the maximum K obtainable is

$$K_{MAX} = (2/r_S)^{1/2} \qquad (5.7)$$
$$r_S \neq 0$$

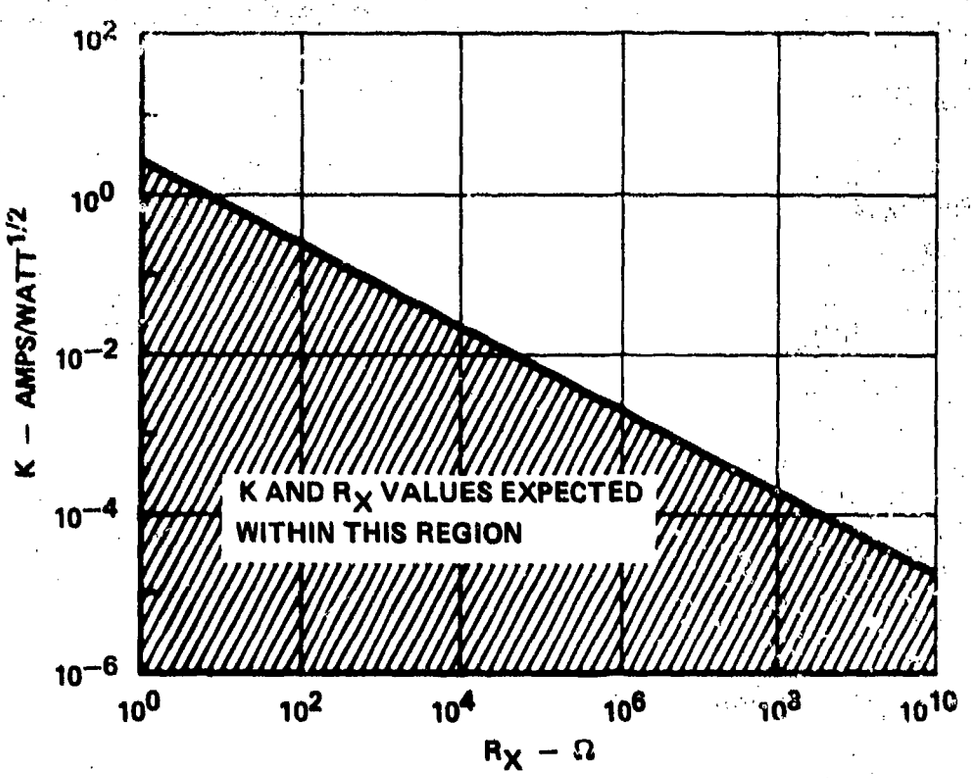


Figure 5.2. Range of Parameters of Junction Model

which occurs at

$$R_X = (2r_S)/(1 + (2\omega C r_S)^2)^{1/2}.$$

Likewise, there exists a minimum value of $R_X(=r_S)$ and a maximum value of $R_X(=1/r_S(\omega C)^2)$.

Figure 5.3 illustrates the implications that the various diode model parameter possibilities have on circuit modeling. Three cases are shown in Figure 5.3(a) as possible values of K and R_X depending upon the values of the RF driving impedances. The value of K is chosen constant in this example, while the value of R_X differs in each of the three cases. Figure 5.3(b) shows the piece-wise linear IV characteristics for the three values of K and R_X chosen. Similar curves result if exponential diodes are assumed. For worst-case circuit analysis, an iterative procedure of selecting possible K and R_X values followed by evaluation of circuit effects may be required. Such a procedure is illustrated in Section 5.4.

Additional information on rectification in PN junctions and the junction rectification model can be found in Reference 13.

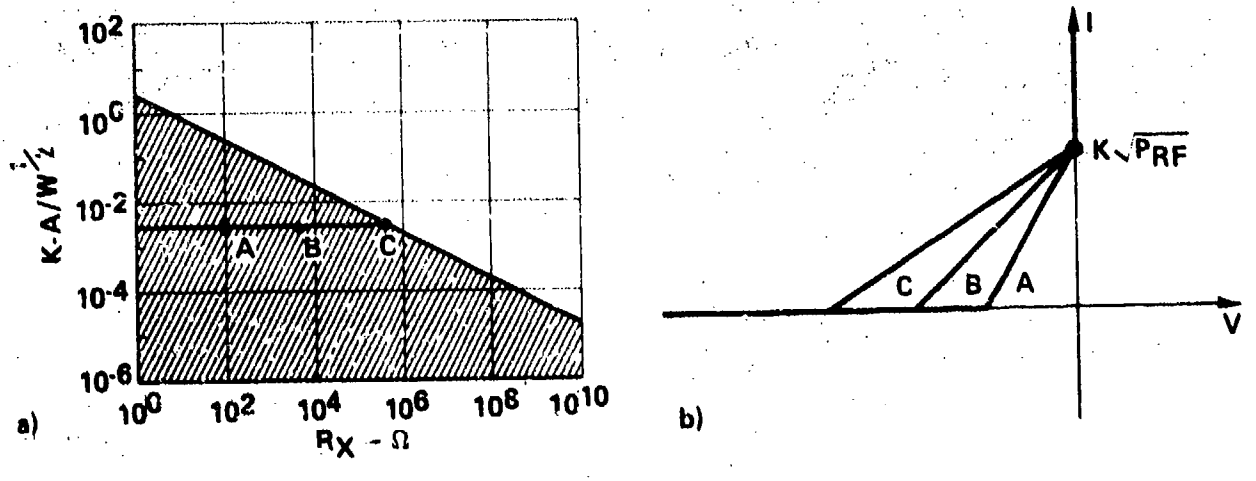


Figure 5.3. Illustration of Relationship Between Possible Choices of Rectification Parameters and Ideal Diode IV Characteristics.

5.2 Interference in Transistors

Transistors, like diodes, experience current and voltage offsets as a result of rectification of RF signals in the transistor junctions. A bipolar transistor contains two PN junctions, and rectification can occur simultaneously in both. The amount of rectification occurring in each junction depends on the junction bias levels and the point of entry of the RF. Additionally, transistors may experience beta changes due to RF energy. Richardson[14] has explained these as due to RF induced current crowding in the transistor emitter.

An existing transistor model, the Ebers-Moll representation, was modified to account for the RF effects in transistors. The Ebers-Moll model is a widely used large-signal transistor model that includes the nonlinear effect of the transistor junctions. As such, it is accurate in all regions of operation: saturation, cutoff, forward active, and reverse active regions. The standard Ebers-Moll model was modified to include rectification effects by substituting the junction rectification model (Figure 5.1) for each of the transistor junctions in the Ebers-Moll model. Figure 5.4 shows the modified Ebers-Moll model. The characteristics of diodes D_{C1} and D_{E1} are given by

$$i_{DC1} = I_{CS}(\exp(qv_{BC}/kT) - 1) \tag{5.8}$$

$$i_{DE1} = I_{ES}(\exp(qv_{BE}/kT) - 1) \tag{5.9}$$

where I_{ES} and I_{CS} are the diode reverse saturation currents,

q is the electron charge,

k is Boltzmann's constant, and

T is the junction temperature in degrees Kelvin.

For simplicity, the characteristics of diodes D_{C2} and D_{E2} are assumed similar to diodes D_{C1} and D_{E1}, respectively. The transistor's forward and reverse betas, β_F and β_R, are related to the values of α_F and α_R by the following relations:

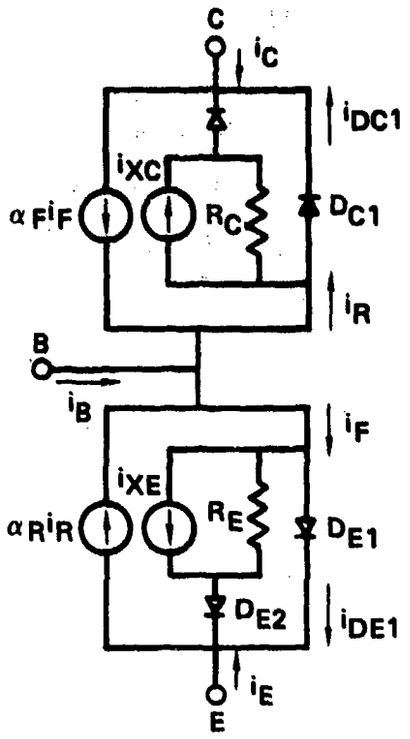


Figure 5.4. Modified Ebers-Moll Model for a Transistor Under RF Influence

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{5.10}$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R} . \tag{5.11}$$

As in the diode rectification model, current sources i_{XE} and i_{XC} are dependent on the RF power level, frequency, and RF source impedance. For large RF signals, they are proportional to the square root of the RF power level, as follows:

$$i_{XE} = K_E\sqrt{P_{RF}} \tag{5.12}$$

$$i_{XC} = K_C\sqrt{P_{RF}}, \tag{5.13}$$

where K_E and K_C are constants which depend on the frequency and source impedance of the interfering RF signal. In general, K_E and K_C decrease with increasing RF

frequency. The values of R_E and R_C are constants with RF power at a given RF source impedance and frequency. The values of R_E and R_C are expected to increase with increasing source impedance or frequency. The ranges of parameters R_E and K_E, and R_C and K_C are given by Figure 5.2. Beta decreases are included in the model by making α_F and α_R functions of the RF power level. In general, α_F and α_R will also be functions of frequency and RF entry port. Figure 5.5 illustrates the total observed range of forward alphas for several transistors for frequencies from 220 MHz to 3 GHz. In general, the greatest decrease occurs at the lower frequencies.

The modified Ebers-Moll transistor model has been used successfully to simulate interference effects in integrated circuits. The model is compatible with existing computer-aided analysis programs, and has been used with the program SPICE and the timesharing version ISPICE without difficulty. Sections 5.3 through 5.5 of this chapter illustrate the use of the model in evaluating interference in integrated circuits. Additional information on the transistor model is contained in Reference 13.

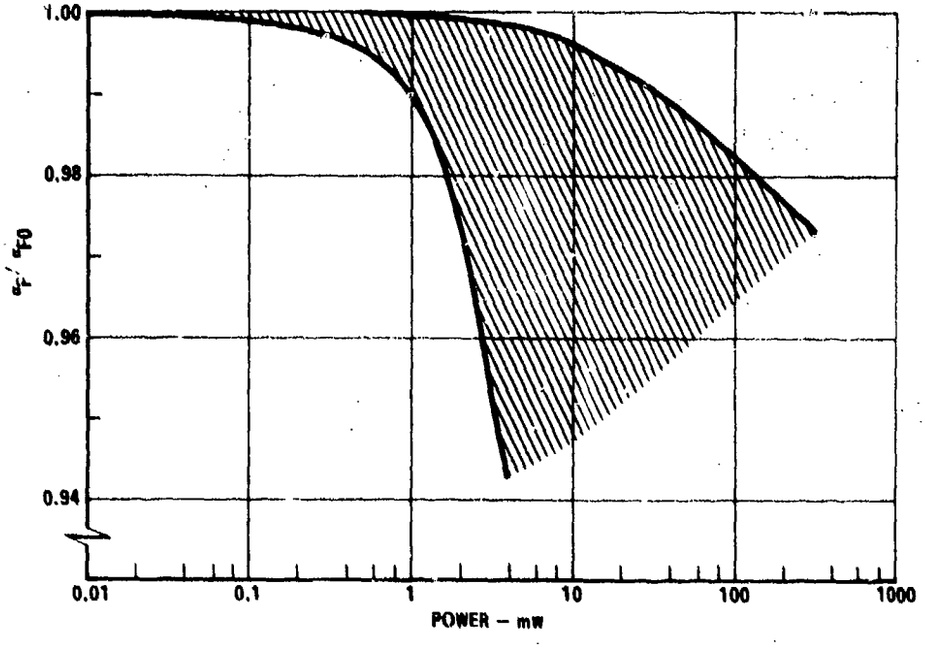


Figure 5.5. Observed Range of Normalized Transistor Alpha With RF Into the Base for Frequencies From 0.22 GHz to 3 GHz

5.3 Computer-Aided Analysis of Circuit Interference

The modified Ebers-Moll transistor model described in the preceding section can be used with electronic circuit analysis programs to provide useful information about interference effects in bipolar integrated circuits. In this section, the program SPICE (Simulation Program with Integrated Circuit Emphasis) is used to simulate interference effects in a 7400 NAND gate, a widely used TTL device.

The electronic circuit analysis program SPICE was developed specifically for analyzing integrated circuits under normal conditions when no interfering signals are present. It is commonly used by circuit designers, integrated circuit manufacturers, and universities. Reference 15 describes the program, its availability and its input code. The program can be used to predict interference effects in integrated circuits using the procedures described in this section. No change in the existing SPICE program code is necessary. Standard SPICE models are used for all components not affected by the RF. The transistors and diodes which are affected by RF are modeled with the transistor and diode models described in the previous sections.

The 7400 NAND gate was selected for this example because it is a common digital IC and because its EM susceptibility properties have been extensively measured and reported upon[16]. Results of these investigations show the 7400 NAND gate is most susceptible to RF conducted into its output terminal when the normal output voltage VOUT is low (VOUT < 0.4). The output voltage is low when both input voltages VIN are high (VIN > 2.0V). RF signals conducted into the output terminal can cause the output voltage to change from a normal low state to an RF induced high state. A NAND gate with RF signals conducted into the output is shown in Figure 5.6. This is the situation that was simulated using SPICE. It should be noted that most members of the 74XX TTL family have essentially identical output circuitry so the results obtained for the 7400 NAND gate should be applicable to other 74XX IC's as well.

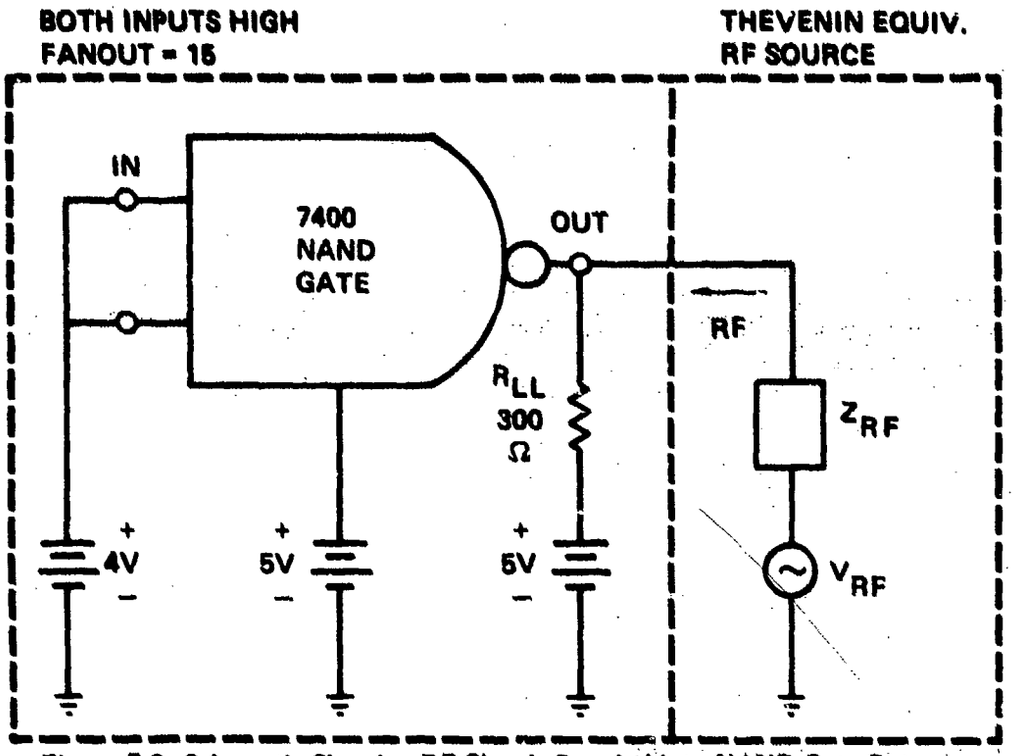


Figure 5.6. Schematic Showing RF Signals Coupled into NAND Gate Output.

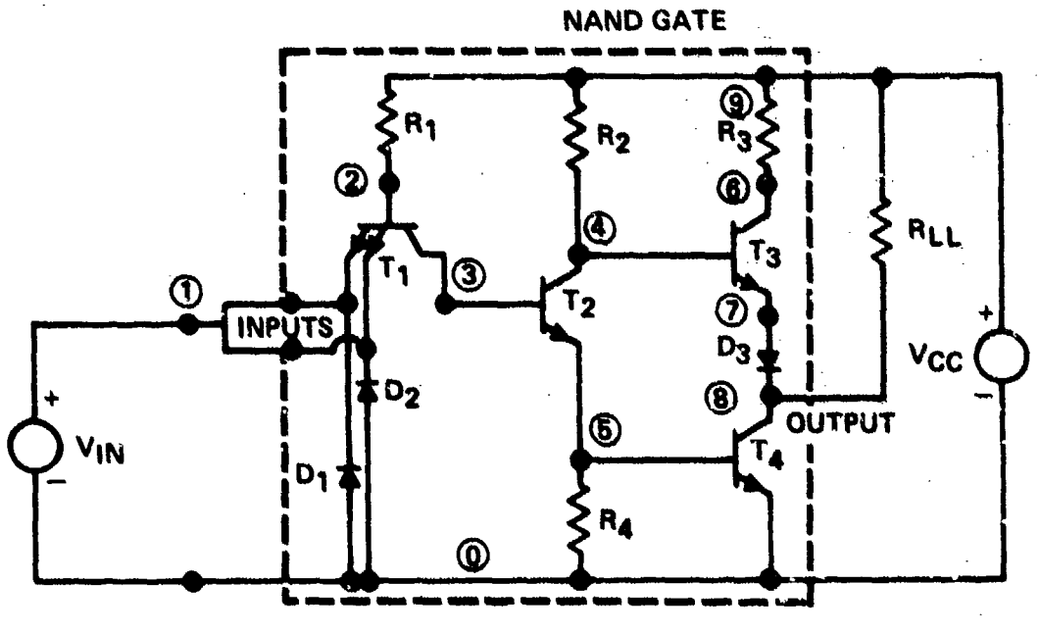


Figure 5.7. Schematic Diagram of 7400 NAND Gate with External Connections. Node Numbers for SPICE Simulations are Shown.

A schematic diagram of a 7400 NAND gate with external connections is shown in Figure 5.7. The dual emitter transistor T1 was modeled by a single emitter transistor, and diodes D1 and D2 were modeled by a single diode DIN. Previous analysis had shown that when RF is injected into the 7400 NAND gate output (as shown in Figure 5.6) the interference effect can be accounted for by assuming all of the RF power is incident on the output transistor T4[17]. Transistor T4 is modeled using the modified Ebers-Moll model shown in Figure 5.4, while all other NAND gate components are modeled using the standard component models available in SPICE.

Parameters for the transistors and diodes in the 7400 NAND gate are listed in Table 5.1. These values were obtained from Reference 18 and were converted into a form usable by SPICE. These parameter values are entered as data for a SPICE simulation. (See Table 5.2 for an example of data for a SPICE simulation of an RF perturbed 7400 NAND gate).

Table 5.1. Diode and Transistor Parameter Values for the 7400 NAND Gate

DIODE PARAMETERS

NAME	PARAMETER DESCRIPTION	DIN	D3
RS	OHMIC RESISTANCE (Ω)	60	30
IS	SATURATION CURRENT (pA)	100	5

TRANSISTOR PARAMETERS

NAME	PARAMETER DESCRIPTION	T1	T2	T3	T4
BF	FORWARD BETA (βF)	.316	19.8	17.2	21.7
BR	REVERSE BETA (βR)	.0024	.060	.082	.106
RB	BASE OHMIC RESISTANCE (Ω)	68	75	70	80
IS	SATURATION CURRENT (pA)	.5	3	8	20
AF[a]	FORWARD ALPHA (αF)	.24	.952	.945	.956
AR[a]	REVERSE ALPHA (αR)	.0024	.057	.076	.0956
IES[a]	EMITTER DIODE SAT. CURRENT (pA)	2	3	8	20
ICS[a]	COLLECTOR DIODE SAT. CURRENT (pA)	200	50	100	200

[a]PARAMETER USED IN MODIFIED EBERS–MOLL MODEL.

Table 5.2. Data Cards for a SPICE Simulation of an RF Perturbed 7400 NAND Gate

```
VCC 9 0 DC 5
VIN 1 0 DC 4.25
VGEN 16 0
 *NODE 0 = NODE 20
R1 9 2 4.38K
R2 9 4 1.43K
R3 9 6 0.116K
R4 5 0 1.06K
RLL 8 9 9.11K
QT1 3 2 1 MOD1
QT2 4 3 5 MOD2
QT3 6 4 7 MOD3
XT4 8 5 0 16 RF-EBML
DIN 0 1 MOD5
D3 7 8 MOD6
 .MODEL MOD1 NPN .316 .0024 68
   IS=5E-13
 .MODEL MOD2 NPN 19.8 .060 75
   IS=3E-12
 .MODEL MOD3 NPN 17.2 .082 70
   IS=8E-12
 .MODEL MOD4 NPN 21.7 .106 80
   IS=2E-11
 .MODEL MOD5 D RS=60 IS=1E-10
 .MODEL MOD6 D RS=30 IS=5E-12
 .DC TC VGEN .2 20 .2
*BY CAUSING VGEN TO VARY THE
*CURRENT GENERATORS ISCC AND ISCE
*WHICH DEPEND UPON THE VOLTAGE ACROSS
*RSWEEP ALSO VARY, THIS SIMULATES
*A CHANGE IN INCIDENT RF POWER.
 .OUTPUT VOUT 8 0 PLOT DC 0 5
 .TEMP 20
*MDAC RF MODIFIED EBERS-MOLL MODEL
 .MODEL RF-EBML X 8 5 20 16
IAFIE V 8 12 12 13 0.956
IARIC V 20 12 12 11 0.0956
RBB 5 12 80
RCSENSE 12 11 1
RESENSE 12 13 1
DC1 11 8 MOD7
DE1 13 20 MOD8
 .MODEL MOD7 D IS=200P
 .MODEL MOD8 D IS=20P
*RF INDUCED TERMS (ELEMENTS)
RSWEEP 16 20 1
RGC 8 10 190
RGE 14 20 180
ISCC V 10 8 16 20 3.79M
ISCE V 14 20 16 20 0.667M
DC2 11 10 MOD7
DE2 13 14 MOD8
 .FINIS
 .END
```

Transistor T4, into which all the RF power is assumed injected, is modeled in SPICE using the modified Ebers-Moll model shown in Figure 5.8. It is incorporated in the SPICE input data as an external model. (For a detailed description on using external models in the program SPICE, see Reference 15). To implement the current-dependent current sources IAFIE and IARIC in the modified Ebers-Moll model, 1Ω current sensing resistors are placed in the emitter and collector as shown in Figure 5.8. The current sources IAFIE ($\alpha_F I_F$) and IARIC ($\alpha_R I_R$) are made to depend upon the voltage drops $V_{12} - V_{13}$ and $V_{12} - V_{11}$ across resistors RESENSE and RCSENSE respectively. The result is that IAFIE = AF($V_{12} - V_{13}$) and IARIC = AR($V_{12} - V_{11}$) where the values for AF and AR (α_F and α_R) are given in Table 5.1. Diodes DE1 and DE2 both have saturation current IES and diodes DC1 and DC2 both have saturation current ICS given in Table 5.1.

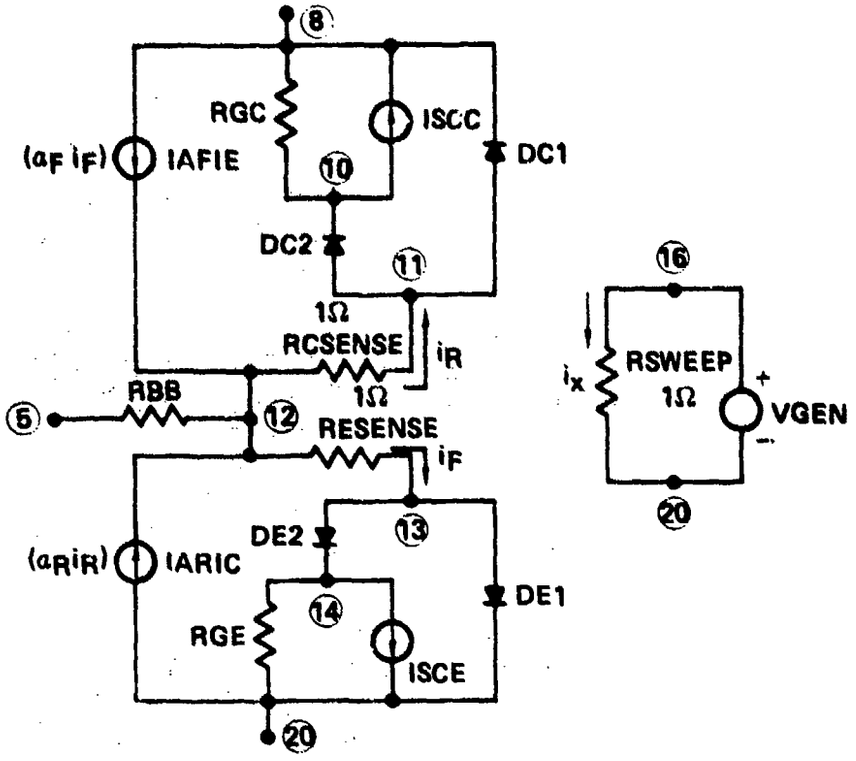


Figure 5.8. Modified Ebers-Moll Model in an External Model Configuration. Node Numbers for SPICE Simulations are Shown.

Also shown in Figure 5.8 is a dc voltage source with value VGEN. The dc voltage source controls the voltage $V_{16} - V_{20}$ which controls the RF induced dc current generators ISCE and ISCC. By causing VGEN to vary over an appropriate range, the values for ISCE and ISCC are made to vary also. This is how the RF power is swept in the computer simulations. The appropriate range of values for VGEN is determined from the relationship

$$P_{INC} = VGEN^2/400\Omega, \tag{5.14}$$

where PINC is the RF power incident on the 7400 NAND gate. The value for PINC is assumed equal to the maximum available power from a Thevenin equivalent RF source of amplitude VGEN and impedance 50Ω. Equation (5.14) may be rewritten as

$$VGEN = (400\ PINC)^{0.5} \tag{5.15}$$

The two RF induced dc current generators ISCE and ISCC depend on VGEN:

$$ISCE = (KE/RGE)VGEN \tag{5.16}$$

$$ISCC = (KC/RGC)VGEN \tag{5.17}$$

The values of KE, KC, RGE and RGC were determined experimentally at 220 MHz for a 2N2369A transistor, which is believed similar to the output transistor T4 in the 7400 NAND gate. The values determined were KE = 0.12, KC = 0.72, RGE = 180Ω, RGC = 190Ω, KE/RGE = 0.067 m℧ and KC/RGC = 3.79 m℧. The ratios (KE/RGE) and (KC/RGC) are effectively transconductances which relate the RF induced dependent current generators ISCE and ISCC to the control voltage VGEN. VGEN is related to the RF incident power by Equation (5.15). Varying VGEN over the range 0.2 to 20V corresponds to varying PINC over the range 0.1 to 1000 mW. (A different procedure to relate ISCE and ISCC to PINC is described in the next section).

Three types of TTL NAND gates were investigated to determine their relative susceptibilities to RF interference. These are the normal 7400 series, the high speed 74H00 series, and the low power 74L00 series. The three NAND gate series use different values of internal resistances R1-R4 shown in Figure 5.7. The resistance values are given in Table 5.3. The three NAND gate types have the same output stage, but resistance R1 in the input stage varies. The variation in the values for R1 affects the value of the resistor RLL required to simulate different fanout values. The values of RLL required to give a low fanout (F = 1) and a high fanout (F = 10 or 15) are also given in Table 5.3.

Table 5.3. Resistor Values for 7400 NAND Gate Type Variations

RESISTOR (kΩ)	7400	FAN-OUT	74H00	FAN-OUT	74L00	FAN-OUT
R1	4.38		2.80		40	
R2	1.43		0.70		20	
R3	0.116		0.116		0.116	
R4	1.06		1.06		12	
RLL	4.38	1	2.80	1	40	1
RLL	0.30	15	0.28	10	4	10

Figure 5.9 shows the predicted values of the NAND gate output voltage VOUT plotted versus the incident RF power PINC. The plots show the relative susceptibilities of the three NAND gate types with low and high fanouts. When no RF power is applied, the output voltage is low (approximately 0.1V). As the RF power increases, the VOUT values increase until they cross the two susceptibility threshold levels. The threshold at VOUT = 0.8V corresponds to the upper allowed

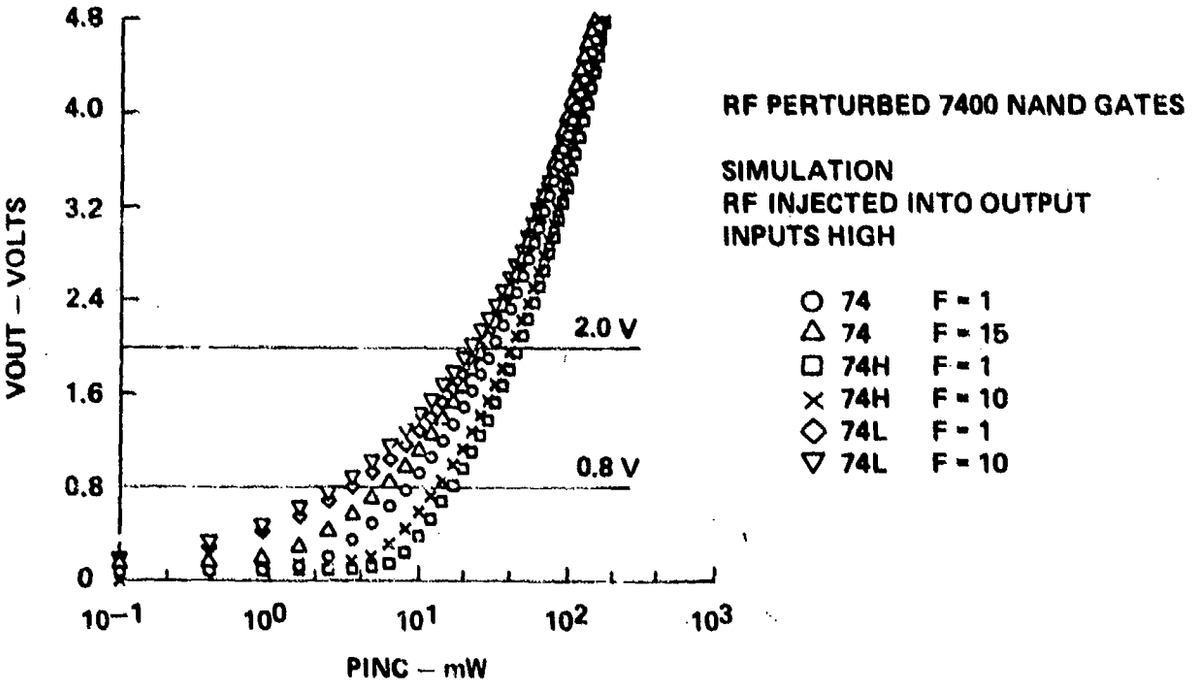


Figure 5.9. Output Voltage vs. Incident RF Power From SPICE Simulations of Three 7400 NAND Gate Types with Different Fanouts. Susceptibility Thresholds at V_{OUT} Equals 0.8 and 2.0 Volts are Shown.

voltage that a subsequent stage is guaranteed to recognize as a low state input. The value VOUT = 2.0V corresponds to a VOUT certain to be recognized as a high state (instead of a low state) by a subsequent TTL input. The values of RF power which cause these two threshold levels to be expected are given in Table 5.4.

Table 5.4. Values of RF Power Which Cause EM Susceptibility Criteria To Be Exceeded for Three 7400 NAND Gate Types

TYPE OF GATE	VOUT = 0.8V		VOUT = 2.0V	
	SPICE[a] P_I (mW)	EXP.[b] P_A (mW)	SPICE[a] P_I (mW)	EXP.[b] P_A (mW)
74L00 (F=10)	2.8		22	
74L00 (F=1)	3.5		25	
7400 (F=15)	5.8	4.0	28	28
7400 (F=1)	7.9		30	
74H00 (F=10)	13		40	
74H00 (F=1)	17		45	

[a]VALUES OF INCIDENT RF POWER.

[b]VALUES OF ABSORBED RF POWER. – SEE REF. 17.
VALUES OF INCIDENT RF POWER WOULD BE HIGHER.

The SPICE simulation results presented in Table 5.4 indicate that the low power 74L00 series NAND gate are the most susceptible to RF interference, while the high speed 74H00 series are the least susceptible. For each NAND gate type the fanout value has a small effect (less than 2 dB difference between minimum and maximum fanout) upon the RF power required to cause the threshold levels to be exceeded. Also given in Table 5.4 are experimental values for the absorbed RF power required to cause the 7400 series NAND gate output voltage to exceed the two susceptibility threshold levels[17]. These experimental values are in good agreement with the values predicted by the SPICE simulations. This agreement indicates that an electronic circuit analysis program such as SPICE can be used to predict RFI effects in digital bipolar integrated circuits quite well. Additional information on simulating NAND gate interference using SPICE can be found in References 17 and 19, and in the next section.

5.4 Worst Case Analysis of Circuit Interference

In the previous section the impedance of the RF generator connected to the 7400 NAND gate was assumed to be 50Ω. The main reason for making this assumption

was to permit a comparison of the SPICE simulation results with experimental results obtained by injecting RF power into a 7400 NAND gate from an RF generator with 50 ohms internal impedance. In an actual interference environment, electromagnetic fields induce RF voltages and currents on wires and cables which are connected to electronic equipment. An induced RF signal can be represented by a Thevenin equivalent containing an RF voltage source of amplitude V_{RF} and an impedance Z_{RF}. This section describes a worst case analysis procedure which can be used when the RF source impedance Z_{RF} is not known a priori.

As in the previous section, the 7400 NAND gate is used as an example with RF conducted into the output terminal as shown in Figure 5.6. Both inputs are assumed to have a high state voltage, and the output voltage is a low state in the absence of RF. As before, the RF is assumed to affect transistor T4 only. The method used to assign values to the RF interference parameters in the modified Ebers-Moll transistor model differs from that used in the previous section. The new method assigns values to ISCE, ISCC, RGE and RGC based on expected ranges of these parameters found for ideal diodes in Section 5.1.

When RF power is injected into the collector of a transistor biased as T4 in the 7400 NAND gate, the worst case simulations are obtained when all of the RF power is assumed to affect the collector-base junction, and none is assumed to reach the emitter-base junction[17]. Thus, no rectification occurs in the emitter-base junction. Rectification in this junction is removed from the modified Ebers-Moll model by setting ISCE = 0 and RGE = ∞. The collector-base junction rectification parameters are assigned with the aid of Figure 5.2. The value of RGC (corresponding to R_χ in Figure 5.2) was swept over the range of 5 to 5000 ohms. (The range 5 to 5000 ohms was chosen somewhat arbitrarily to give a worst case response. In certain situations a wider range may be necessary.) The value of K_C was chosen as the

upper line of Figure 5.2, which gives

$$K_C = (C/RGC)^{1/2} \tag{5.18}$$

where

$$ISCC = K_C(PINC)^{1/2}. \tag{5.19}$$

If we choose

$$PINC = VGEN^2/8\ RGC, \tag{5.20}$$

then from Equations (5.18) and (5.19),

$$ISCC = VGEN/RGC. \tag{5.21}$$

The program SPICE was used to perform a worst case analysis of the 7400 NAND gate. The value of external resistor RLL was set to 300Ω, corresponding to a fanout of 15. (Results of the previous section indicate that high fanouts lead to EM susceptibility at slightly lower RF power levels than low fanouts). The first step in the simulation procedure is to assign a value for the resistance RGC in the collector-base junction of T4. The range of 5 to 5000 ohms was simulated in the SPICE runs. The next step is to sweep the dc control voltage VGEN in the SPICE program over an appropriate range of voltages corresponding to the desired range of incident RF powers, as given by Equation (5.20). At each value of VGEN, the value ISCC is given by Equation (5.21). As a final step, the values of the output voltage VOUT can be plotted versus PINC. Then the process is repeated using a new value of RGC until adequate coverage of the entire range of RGC has been obtained.

Figure 5.10 plots VOUT versus PINC from SPICE simulation results using RGC in the range of 5 to 5000 ohms. Observe that the value of RGC is quite influential in determining the shape of the VOUT versus PINC curve, and in determining the RF power levels at which various EM threshold levels are crossed. From Figure 5.10, the values of incident power required to cause VOUT to cross EM susceptibility threshold levels of 0.4, 0.8, and 2.0 volts were determined for each simulation. These values

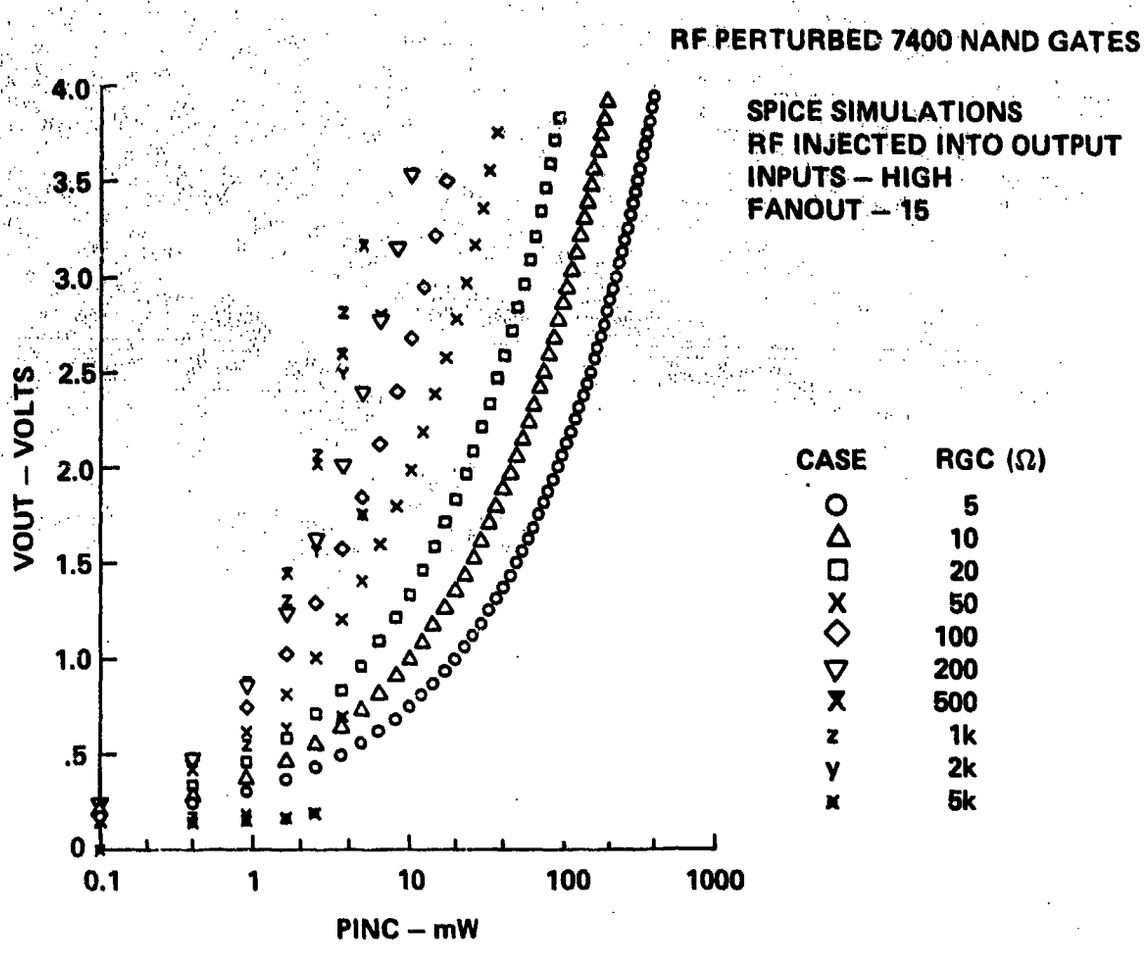


Figure 5.10. SPICE Simulation Values of Output Voltage versus Incident RF Power Level for a 7400 NAND Gate

are plotted in Figure 5.11 versus the value of RGC for that case. Three curves result: one for each threshold level. It is observed from Figure 5.11 that for each susceptibility threshold level that the PINC versus RGC plot has a minimum PINC value. The minimum values of PINC provide a usable estimate of the minimum incident RF power expected to cause the various EM susceptibility threshold levels to be exceeded. (The location of these minima is the primary purpose of the worst case modeling. The range of RGC used should include the values that produce minima in the PINC vs RGC curves or, alternatively, an iterative procedure can be used to locate these minima). Notice that the minima for the three threshold level do not occur at

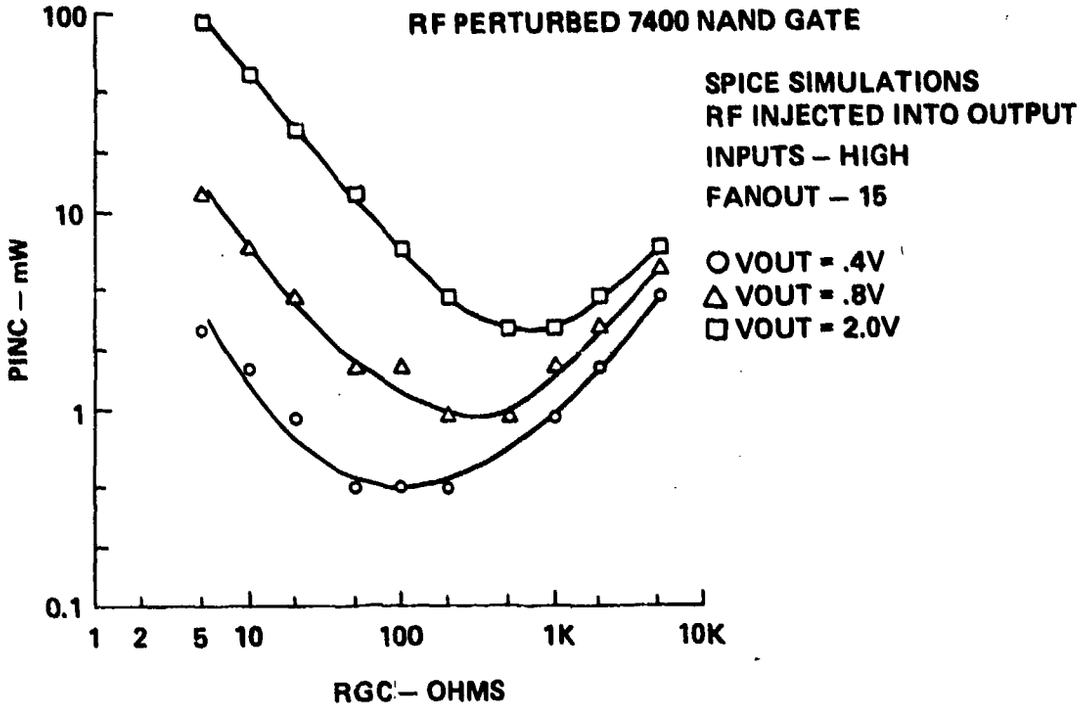


Figure 5.11. Values of Incident RF Power Required to Cause Output Voltage of 7400 NAND Gate to Exceed Susceptibility Threshold Levels versus the RF Thevenin Source Impedance

the same value of RGC. The resulting minimum susceptibilities predicted for thresholds of 0.4, 0.8, and 2.0 volts are plotted in Figure 4.2 versus frequency (a constant of proportionality was used to convert the predicted incident power values to absorbed power for Figure 4.2). Since the impedance of the Thevenin RF source in Figure 5.6 was assumed completely arbitrary, in the worst case, no frequency dependence enters the predicted susceptibility data.

The predicted worst case curves in Figure 4.2 lie below the measured worst case curves. This is reasonable, since the SPICE simulations analyzed a wider range of RF conditions than could reasonably be studied in the laboratory. Additionally, several conservative assumptions were made in the analysis: all of the interference effect is in the collector-base junction of T4, no loss exists in the collector-base junction, etc. The RF impedances used in the simulations included those typically encountered in actual interference environments. It is unlikely

that RF powers below the predicted susceptibility levels will cause interference in any real-world application.

The worst case analysis procedure described in this section is quite general and can be applied to other electronic circuits or IC's. Comparison of the predicted worst case results for the 7400 NAND gate with the worst case results measured in the laboratory gives confidence that such a simulation procedure is valid.

5.5 Interference Analysis Using Macromodels

Models of interference in the 741 op amp have been studied for the case of RF conducted into the input terminals. Macromodeling techniques were used to model the op amp and the modified Ebers-Moll transistor model was used to account for the interference effect, which was assumed to occur only in a single input transistor. This section describes the analysis of interference in a 741 op amp.

The op amp macromodel used was previously published by Boyle, et. al[20], and is illustrated in Figure 5.12. Much of the internal structure of the op amp has been

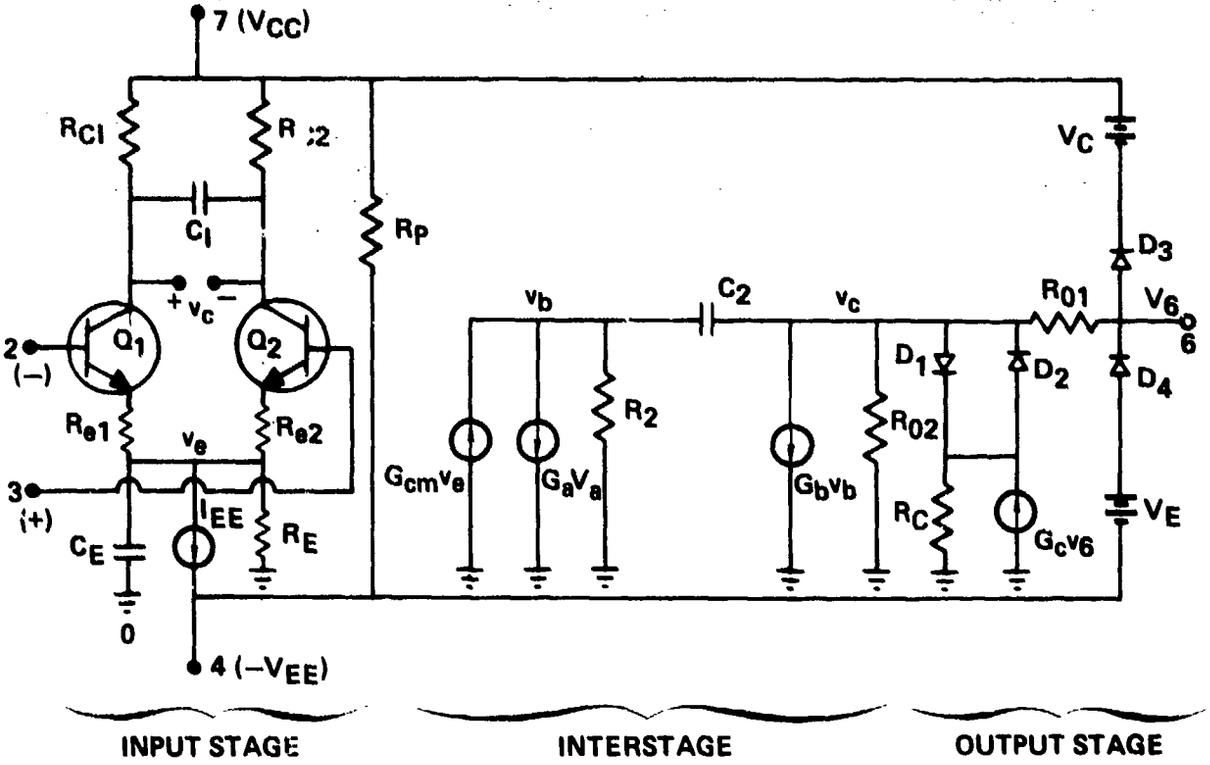


Figure 5.12. 741 Op Amp Macromodel

replaced with functional equivalents. This reduces the amount of computer time required to obtain a solution, because the macromodel has fewer elements than the operational amplifier, and because much of the circuit consists of linear elements, instead of nonlinear elements such as transistors and diodes. Terminally, however, the op amp macromodel behaves like an actual op amp. Table 5.5 lists the macromodel parameters.

Table 5. 5. Macromodel Parameters for LM 741

T	300°K
I_{SD3}	8×10^{-16}A
R_2	100 kΩ
C_2	30 pF
C_E	2.41 pF
β_1	150 (NO RF)
β_2	150 (NO RF)
I_{EE}	20.26 μA
R_E	9.872 MΩ
R_{C1}	5306 Ω
R_{e1}	2712 Ω
C_1	5.460 pF
G_a	188.6 μmho
G_{CM}	6.28 nmho
R_{01}	32.13 Ω
R_{02}	42.87 Ω
G_b	247.49 mho
I_{SD1}	8×10^{-16}A
R_C	0.02129×10^{-3} Ω
G_C	49964 mho
V_c	1.803 V
V_E	2.303 V

A significant feature of the macromodel created by Boyle is that it retains the differential pair configuration at the input terminals, as is found in an actual 741. The two transistors at the input of the macromodel perform the same

functions as their counterparts in the actual device. The macromodel uses an Ebers-Moll transistor model for each input transistor.

With RF entering the input of the op amp, it was postulated that the interference effect could be accounted for by replacing the transistor model at that input with a modified Ebers-Moll transistor model (Figure 5.4), which includes RF effects. Figure 5.8 shows the modified Ebers-Moll transistor model used in the simulations. The input transistors were assumed similar to 2N930A transistors in characteristics. RF parameters were inferred from measured 2N930A data. Table 5.6 lists the modified Ebers-Moll parameters at 220 MHz. The effect of decreasing beta for increasing RF power was included in the modified model. Only the transistor at the RF input was modeled with a modified Ebers-Moll model; the other input transistor used a standard Ebers-Moll model having the same parameters (except RF parameters) as the modified model.

Table 5.6. Modified Ebers-Moll Parameters for Op Amp Input Transistors

α_F = 0.993377 (NO RF)

α_R = 0.6666

$I_{DE1} = 5.067 \times 10^{-14} \left(e^{\frac{q}{kT} V_{DE1}} - 1\right)$ AMPS

$I_{DE2} = 3.4 \times 10^{-14} \left(e^{\frac{q}{kT} V_{DE2}} - 1\right)$ AMPS

RGC = 1KΩ

RGE = 100Ω

ISCC = $0.01\sqrt{P_{RF}}$ AMPS

ISCE = $0.17\sqrt{P_{RF}}$ AMPS

WHERE P_{RF} IS RF POWER IN WATTS.

The op amp was simulated in a feedback amplifier circuit with a gain of -10. Figure 5.13 illustrates the circuit. This corresponds to the circuit used when op

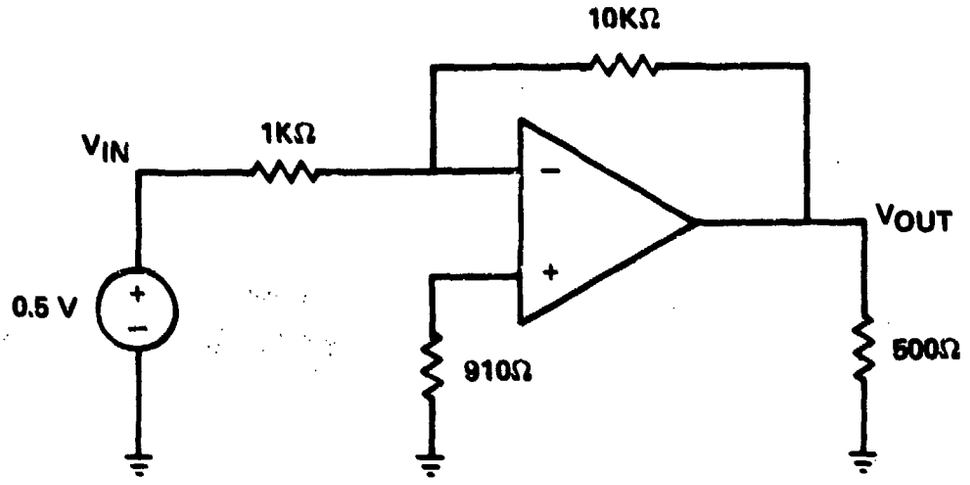


Figure 5.13. Closed Loop Amplifier Circuit Used in Op Amp Simulations

amp susceptibilities were tested in the lab. The input voltage is 0.5 volts, so the expected output voltage with no RF is -5.0 volts.

The circuit was simulated on ISPICE, a timesharing version of the program SPICE which is available through National CSS, Inc. Figure 5.14 is a listing of the input statements for an RF simulation. The input command structure is similar to that used in SPICE, but several additional features are available. One example is that circuit element values may be made functions of an independent variable. In the listing of Figure 5.14, RFPWR is an independent variable specifying the RF power level. The values of current sources ISCC and ISCE are then made functions of the RF power level with the commands

```
ISCC        4        1        XC(RFPWR)
ISCE        7        3        XE(RFPWR)
```

where XC(RFPWR) and XE(RFPWR) are functions of the RF power level specified by the following statements:

```
XC(RFPWR) = 0.01 * (RFPWR) ** .5
XE(RFPWR) = 0.17 * (RFPWR) ** .5.
```

Another feature available in ISPICE is that element values may be specified in tabular form versus an independent variable. In Figure 5.14, the forward alpha is tabulated versus RF power in the statement

GAFIE 1 2 2 6 TABLE(RFPWR 0, .9933, .125M, etc.)

When executing, the values of the independent variables must be specified, and if desired, they may be stepped over a range of values. The latter procedure was used to obtain values of output voltage vs. the RF power level. Additional information on ISPICE features and command structure can be found in the ISPICE Reference Manual[21].

```
FILE: AMP-741  CKT      FROM: F.DISK

RL 15 0 500
RFB 15 1 10K
RIN+ 0 2 910
RIN- 1 1 1K
RC1 7 5 5305
RC2 7 6 5305
RE1 3 9 2712
RE2 4 9 2712
RE 9 0 9.87OMEG
R2 10 0 100K
RO1 11 15 32.13
RO2 11 0 42.87
RC 12 0 0.02129M
C1 5 4 5.46P
C2 10 11 30P
CE 9 0 2.41P
D1 11 12 DILIM OFF
D2 12 11 DILIM OFF
D3 15 13 DVLIM OFF
D4 14 15 DVLIM OFF
* 'OFF' INDICATES THAT THE ASSOCIATED DIODE IS OFF FOR
*  INITIAL ANALYSIS
XQ1 5 1 3 EB-MOL1
XQ2 6 2 4 RF-EBMOL(RFPWR)
* 'RFPWR' IS THE VARIABLE REPRESENTING THE RF POWER
* 'RFPWR' WILL BE SWEPT OVER A USER DETERMINED RANGE
* 'X' AS THE FIRST LETTER OF AN ELEMENT NAME INDICATES
* A CALL TO A SUBCKT
VIN1 16 0 VIN1
VC 7 13 DC 1.803
VE 14 8 DC 2.303
VCC 7 0 DC 12
VEE 8 0 DC -12
IEE 9 8 DC 20.26U
GCMVE 0 10 9 0 6.28N
GAVA 10 0 5 6 188.6U
GBVB 11 0 10 0 247.49
GCV15 0 12 15 0 46.964K
* ELEMENTS BEGINNING WITH 'G' ARE VOLTAGE CONTROLLED CURRENT SOURCES
MODEL DILIM D(IS=8E-16)
MODEL DVLIM D(IS=8E-16)
ISPICE: >
```

Figure 5.14. List of Input Statements for ISPICE Simulation of 741 Macromodel Including RF Effects

```
FILE: RF-EBMOL SUBCKT   FROM: P
RF-EBMOL(RFPWR)
* 'RFPWR' IS THE VARIABLE REPRESENTING THE RF POWER
* 'RFPWR' WILL BE SWEPT
NODES(1 2 3)
* (1 2 3 ) MUST CORRESPOND TO THE NODES ON THE SUBCKT CALL IN CKT
RCSENSE 5 2 1
RESENSE 6 2 1
ROC 4 1 1K
ROE 7 3 100
GAFIE   1 2 2 6 TABLE(RFPWR,0,.9933,.125M,.9926,.35M,.9906,1.85M,.9474,1
                      4.4M,.9130,19M,.7989)
* ELEMENTS IN THE LIST TABLE ARE OF   E FORM:
* (RFPWR,ALPHA,RFPWR,ALPHA,RFPWR,ALPHA.....)
GARIC   3 2 2 5 0.666
* ELEMENTS BEGINNING WITH 'G' ARE VOLT. CONTROLLED CURRENT SOURCES
ISCC    4 1 XC(RFPWR)
ISCE    7 3 XE(RFPWR)
* 'XC()' AND 'XE()' ARE CALLS TO FUNCTION FILES
* THE FUNCTION FILES DETERMINE THE  AMOUNT OF
* RF POWER INTO THE COLLECTOR AND THE AMOUNT INTO THE EMITTER
DC1     5 1 DC OFF
DC2     5 4 DC OFF
DE1     6 3 DE
DE2     6 7 DE OFF
* 'OFF' INDICATES THAT THE ASSOCIATED DIODE IS OFF FOR .
* INITIAL ANALYSIS
MODEL DC D(IS=5.067E-14)
MODEL DE D(IS=3.4E-14)
ISPICE: >


FILE: EB-MOL1  SUBCKT   FROM: P DISK

EB-MOL1
* STANDARD EBERS MOLL MODEL
NODES(1 2 3)
* (1 2 3) MUST MATCH THE NODES ON THE SUBCKT CALL CARD IN CKT
RBB 2 6 1
RCSENSE 4 6 1
RESENSE 6 5 1
GAFIE   1 6 6 5 .9933
GARIC   3 6 6 4 0.6667
* 'G' INDICATES A VOLTAGE CONTROLLED CURRENT SOURCE
DE1     5 3 DE
DC1     4 1 DC OFF
MODEL DE D(IS=3.4E-14)
MODEL DC D(IS=5.067E-14)
ISPICE: >
```

Figure 5.14. (continued) List of Input Statements for ISPICE Simulation of 741 Macromodel Including RF Effects

Figure 5.15 shows the output voltage of the circuit vs. RF power level when RF enters the inverting input, and compares it to data measured in the laboratory[22]. The output voltage decreases as the input power increases until the amplifier reaches saturation. The simulation data is conservative compared to the measured data by approximately 4 dB. This is reasonable, however, because it was assumed that the incident power affects only the input transistor. In reality, it is unlikely that all of the incident RF power actually reaches the input transistor. Some is probably absorbed in other parts of the chip, or bypasses the input transistor through shunt capacitance. Figure 5.16 plots the output voltage vs RF power when

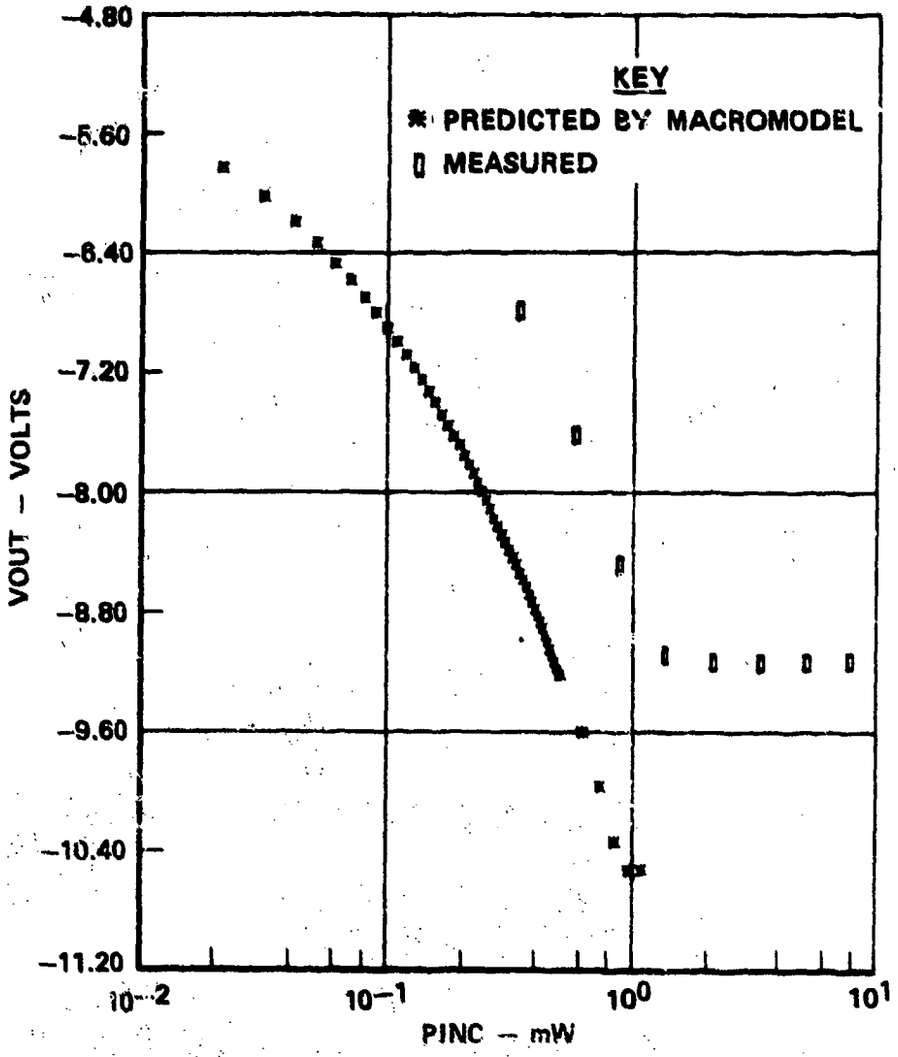


Figure 5.16. Output Voltage of Amplifier Circuit vs. Incident RF Power. RF Conducted into Inverting Input of 741 at 220 MHz.

RF enters the noninverting input and compares it to the measured case. Again, the calculations are conservative by about 4 dB.

The voltage at which the macromodel saturates are different than the saturation voltages actually observed. The macromodel saturates at -10.5 volts and at a voltage greater than +10.5 volts (since, in Figure 5.16, the amplifier has not yet reached saturation at 10.5 volts), where the supply voltages used were $\pm$12 volts. The actual op amp saturates at -9.2 and +10.1 volts. These differences indicate that the values of V_E and V_C, which control the saturation voltage in the macromodel,

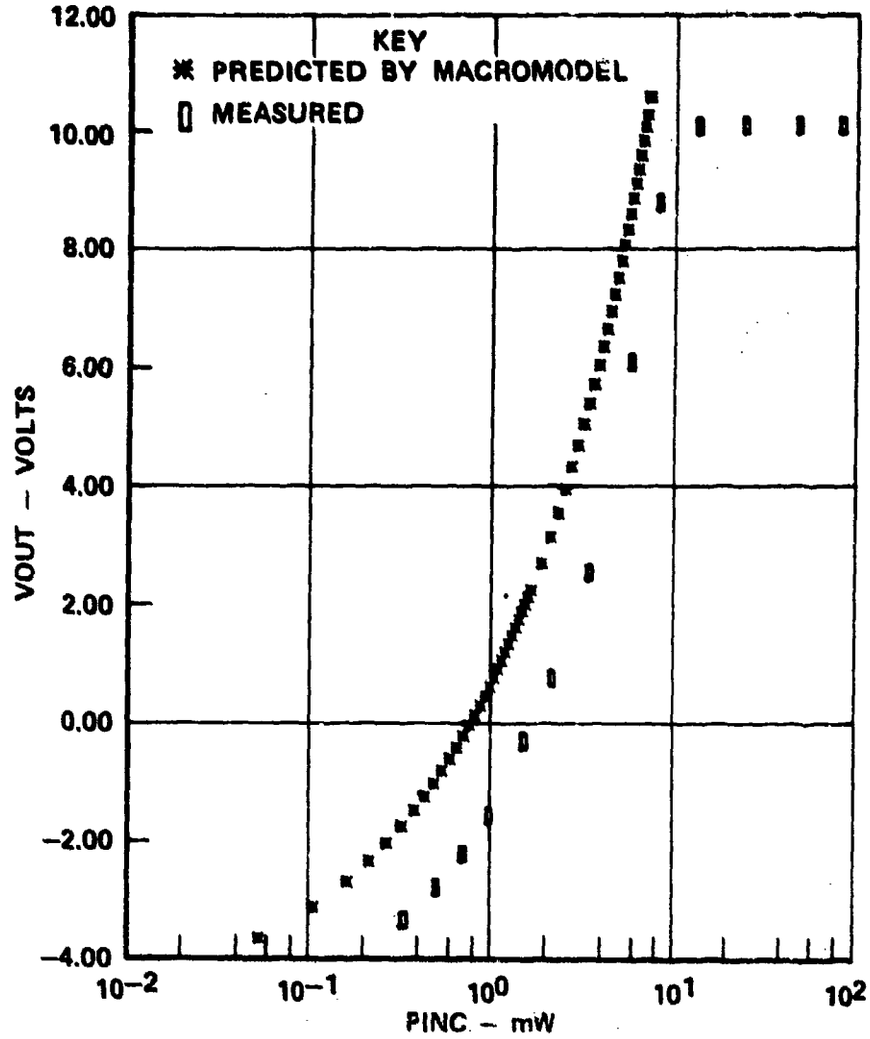


Figure 5.16. Output Voltage of Amplifier Circuit vs. Incident RF Power. RF Conducted into Noninverting Input of 741 at 220 MHz.

should be adjusted if better agreement is desired. The saturation voltages are independent of the interference effects.

In Section 4.5 the simplified op amp interference model shown in Figure 4.9 was presented, where the interference effect is represented by an input offset voltage generator, V_{II}, in series with the input terminals. The relationship between V_{II} and the RF power level would be known, or could be determined mathematically or through measurements. A similar effect is observed in the computer simulations.

In Figure 4.11 an inverting amplifier circuit was shown which is the same as that simulated using ISPICE and which includes the offset generator V_{II} at the op amp inverting input terminal. In Equation (4.2) the output voltage was found to be

$$V_{OUT} = -V_{IN} \frac{R_F}{R_{IN}} - V_{II} \left(\frac{R_F}{R_{IN}} + 1\right). \tag{5.22}$$

In the circuit shown in Figure 5.13, $R_{IN} = 1K\Omega$, $R_F = 10K\Omega$, and $V_{IN} = 0.5V$, so

$$V_{OUT} = -5 - 11V_{II} \text{ volts}. \tag{5.23}$$

Good correlation has been found between the ISPICE calculated output voltage, and the output voltage predicted by Equation (5.23) where the input offset voltage was the product of ISCE and RGE (Figure 5.7). Thus,

$$V_{II} = ISCE * RGE$$

$$= 17\sqrt{P_{RF}} \text{ volts} \tag{5.24}$$

where P_{RF} is the RF power level in watts. A plot of the output voltage using (5.23) and (5.24) is compared in Figure 5.17 with the output voltage from the ISPICE simulations, for the case when RF entered the inverting input. The correlation is found to be excellent. Therefore, the input offset voltage is seen to be the open circuit voltage of the Norton equivalent in the base-emitter junction of the input transistor, which arises from rectification of the RF signal in this junction.

This result can be seen in another way. In the op amp, the input transistors are in a differential pair circuit. Figure 5.18 shows a basic differential pair circuit where the transistors have been replaced by transistor models. RF is assumed to enter the leftmost transistor, so it is modeled with a modified Ebers-Moll model, while the other transistor is unaffected by the RF, so is modeled with a standard Ebers-Moll model. In the op amp, both of the input transistors are biased in an "on" state by the current source I_E which drives the differential pair.

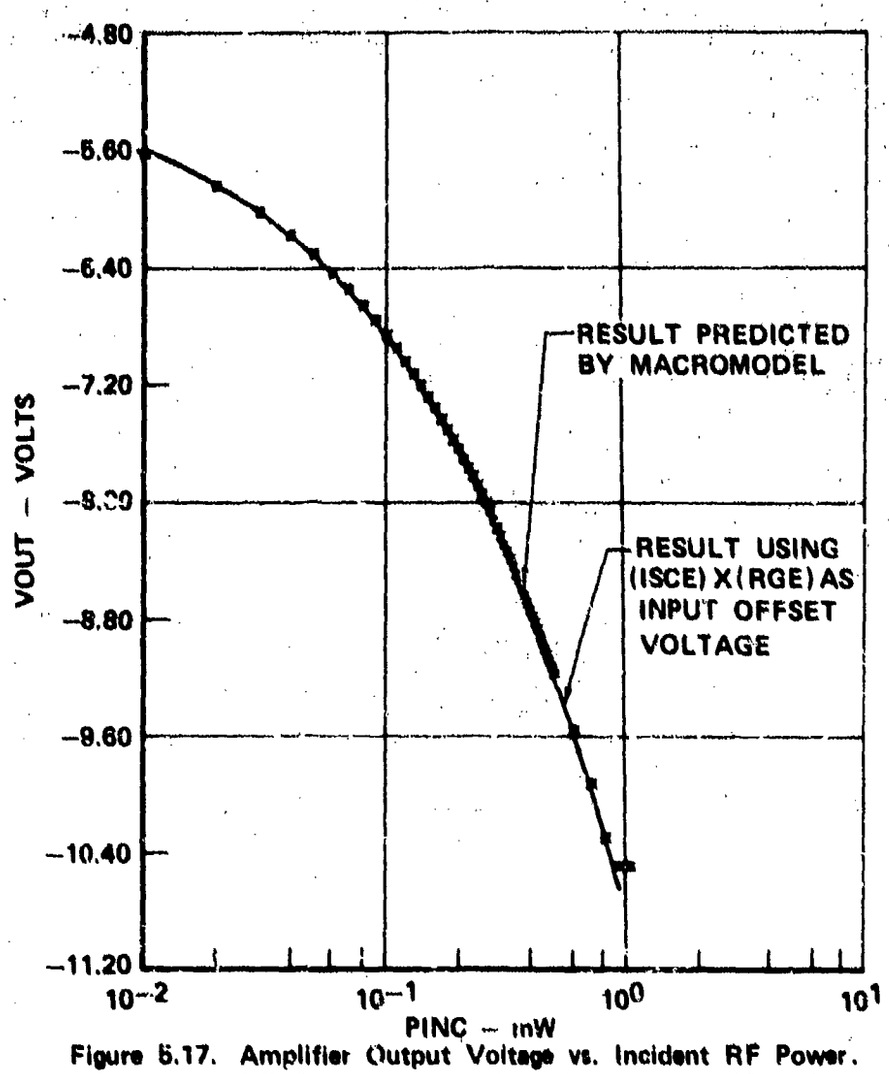


Figure 5.17. Amplifier Output Voltage vs. Incident RF Power. RF Conducted into Inverting Input at 220 MHz.

As such, many of the elements in the transistor models are inactive. Figure 5.19(a) shows the differential pair after removal of the inactive elements. The collector junctions have been removed, since they are reverse biased and do not conduct, and the current controlled current source $\alpha_R I_{R1}$ and $\alpha_R I_{R2}$ have also been removed. In the leftmost transistor, the RF level is assumed large enough so that most of the current I_{F1} flows through diode D_{XE1}, so diode D_{E1} was also removed. In addition, the Norton equivalent I_{XE} and R_{XE} has been replaced with the Thevenin equivalent V_{XE} and R_{XE}, where

$$V_{XE} = I_{XE} R_{XE}. \tag{5.25}$$

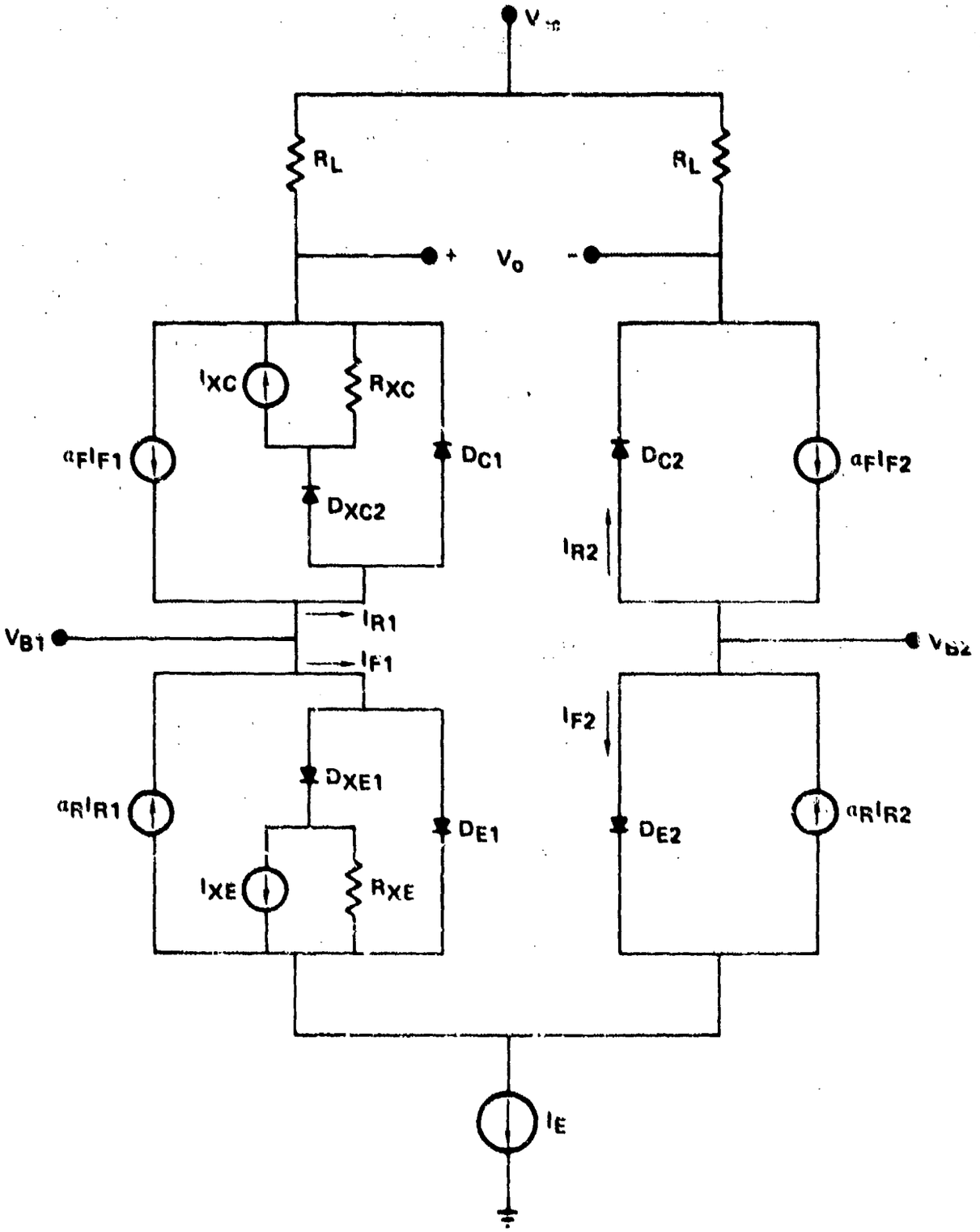


Figure 5.18. Basic Differential Pair Circuit With Transistors Replaced with Ebers-Moll Models. RF Enters Leftmost Transistor.

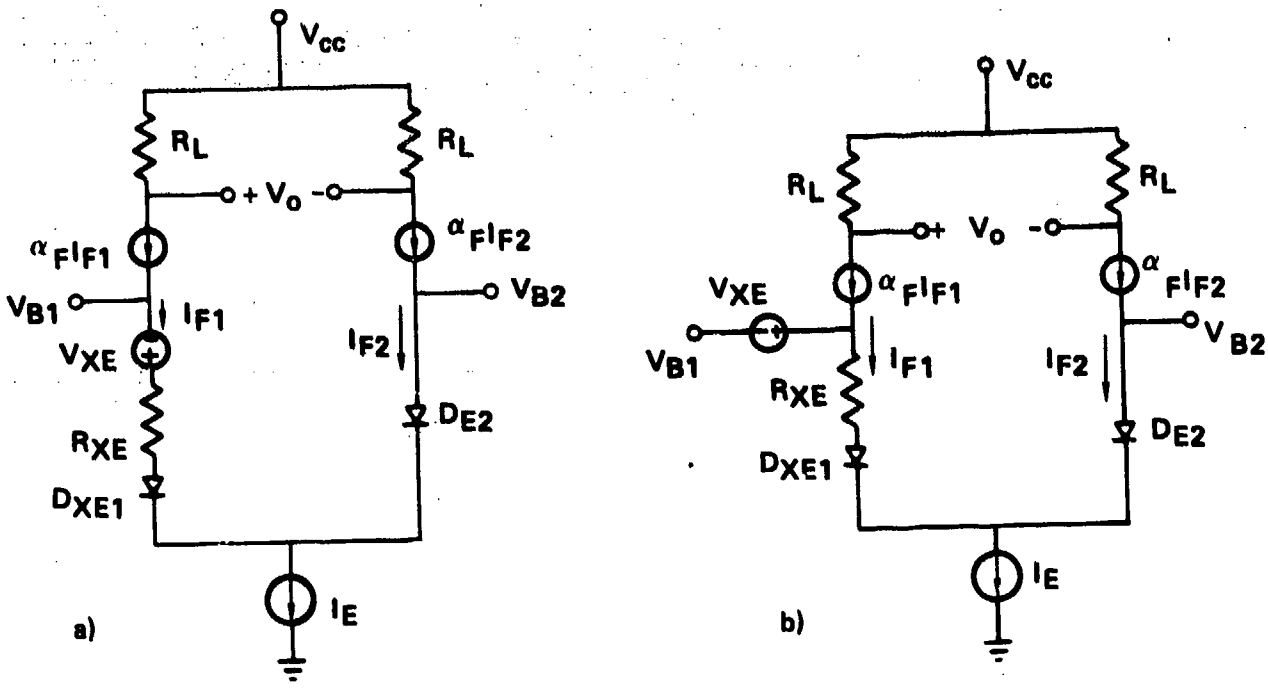


Figure 5.19. Simplification of Basic Differential Pair Circuit. RF Enters Leftmost Transistor.

It is apparent that, because the current source $\alpha_F I_{F1}$ in the left-hand branch of the differential pair can have any voltage across it, the voltage source V_X can be moved into the base lead of the left transistor, as shown in Figure 5.19(b). The offset voltage corresponding to v_{II} in Figure 4.9 is then

$$v_{II} = V_{XE} - I_{F1} R_{XE}. \tag{5.26}$$

The value of $I_{F1} R_{XE}$ is insignificant compared to V_{XE} (remember the RF power level was assumed large enough that most of I_{F1} flows through D_{XE1}, which implies that V_{XE} would be significantly larger than $I_{F1} R_{XE}$). Therefore, the voltage drop across R_{XE} can be neglected. The simplified model shown in Figures 4.9 and 4.11 then follows where

$$v_{II} \approx I_{XE} R_{XE}. \tag{5.27}$$

The macromodeling procedure described in this section has led to a greater insight of the interference effects in op amps, and to verification of a simplified model presented in Section 4.5.

CHAPTER 6

INTERFERENCE REDUCTION TECHNIQUES

While earlier chapters of this handbook addressed the problem of determining whether interference was possible in a given system, this chapter discusses methods of reducing the interference effects. Several methods are discussed. Some of the methods are rather unique to integrated circuits; for example, Section 1 discusses the feasibility of screening integrated circuits to find those devices which are least susceptible to RF energy. Section 2 discusses the use of lossy materials in protecting integrated circuits from RF energy. Section 3 offers suggestions for designing less susceptible circuits. Some of the more common interference reduction techniques (i.e., shielding, gasketing, etc.) are not discussed because numerous references already exist on these subjects.

6.1 Component Screening

The prevention of interference in electronic systems should begin at the earliest stages of design. One step that can be taken early in a program is the selection of less susceptible integrated circuits. This includes selection of device type and manufacturer. During production, further screening can be done to choose those devices from a given lot that exhibit the least interference response. The use of screening, however, should be reserved for the situation where interference problems cannot be resolved with the use of conventional (and less costly) methods.

In choosing an integrated circuit type to perform a specific function, several characteristics should be sought in order to minimize the possibility of interference. Digital IC's with large noise margins are desirable because larger offsets are required before spurious responses occur. Circuits that use high signal levels and high operating currents will experience less upset to unwanted rectified signals.

For example, both measurements and modeling show that low power TTL logic circuits (54L/74L family) are slightly more susceptible than the higher speed, high dissipation circuits (54H/74H family). The difference is small (a few dB), but similar situations occur for many different classes of IC's. Interactions with the surrounding circuit should also be considered. In a voltage-dependent circuit, low impedance IC's and associated circuitry minimize the voltage offsets produced by the rectification process. Similarly, in current-dependent circuits, high impedance IC's and circuitry minimize the current offsets which are produced. Again, this suggests that higher dissipation IC's will be less susceptible than lower dissipation IC's. This is not true in general when comparing two different technologies. In Chapter 4, the susceptibilities of TTL and CMOS digital circuits are reported. The CMOS devices appear less susceptible, even though their dissipation is much less. This occurs because of the wider noise margin of the CMOS family, and is not related to differences in dissipation.

During the course of this study, differences in the susceptibility of devices produced by different manufacturers have been noted. No information is presented in this handbook, however, because this information appears to be reliable only over a short period of time, and may be misleading or incorrect at a later date. Specifically, devices with the same date code appear moderately uniform in susceptibility, but devices with different date codes may be highly different in susceptibilities. This occurs because manufacturers' IC layout designs and processes change whenever increases in performance or economy can be achieved. The resulting devices have the same type number and meet the same specifications as the original devices, but their interference properties may be drastically altered. Where small, limited production projects are planned, and where the designer can be certain of obtaining devices of the same layout and processing (preferably of the same date code), then meaningful device screening by manufacturer could be performed

to reduce the equipment susceptibility. However, it is not recommended that this be attempted for large production projects, or ones in which production (and device procurement) is expected to occur over an extended period of time.

During production, a final screening can be done to select those individual devices from a given lot that have the most desirable interference characteristics. Normal processing variations cause device susceptibilities to vary (often over a range greater than 10 dB) among devices with the same manufacturer and date code. Each device of the lot can be tested, with those individual devices that are the least susceptible being used in the sensitive locations of the electronic equipment. The devices rejected by this screening could be used in locations where interference is not expected to be a problem.

Manufacturer and individual device screening could be accomplished using test techniques similar to those described in Appendix A. Alternatively, simplified test fixtures and measurement systems could be devised to perform limited tests of specific devices at a lower cost and complexity than required for more general, research-type testing. For example, a simple "pass-fail" test might be devised for production screening tests.

Presumably, device screening would be considered only for devices located in extremely sensitive locations in electronic equipment, or where difficulty is anticipated in meeting a given EM environment specification using more conventional methods. The use of shielded enclosures, shielded and twisted pair cables, filters, and EMI gaskets are some of the conventional interference reduction methods that should be exploited before relatively high cost device screening tests are considered.

6.2 Use of Lossy Materials

Lossy materials consist of small iron or ferrite particles embedded in a suitable matrix material such as epoxy or silicone rubber. Such materials are available commercially in a variety of forms including solid stock and castable

liquids. The materials are generally nonconducting, and do not add any low frequency loading to a circuit. They are useful in interference reduction schemes because they can provide considerable insertion loss at microwave frequencies.

In use, the conductor carrying the signal to be attenuated is encased in the material (as closely as possible since the absorption effectiveness falls off with distance from the conductor). The attenuation of the signal depends on the length of the absorbing section and the frequency of the signal. In general, the attenuation increases with increasing length and frequency. Possible uses for lossy materials lie in the fabrication of IC sockets and packages, printed circuit boards, and as a potting material for electronic assemblies.

During this study, the feasibility of using lossy materials was investigated with the fabrication of a lossy IC socket. The socket was made using lossy material in the form of a castable resin. A mold was made from a commercial plastic 16 pin DIP socket, and a reproduction of the socket was cast using the lossy material. The lossy socket was then fitted with the metal contacts taken from the plastic socket. Figure 6.1 is a photograph of the finished ferrite socket. The socket was evaluated at four frequencies using the relative susceptibilities of three different types of ICs. Figure 6.2 shows the protection provided by the socket at three frequencies. At 220 MHz there was no improvement. At the highest test frequency (5.6 GHz), the protection was the highest observed. In some cases at 5.6 GHz, the protection was so high that the change in dc parameters under RF was negligible with the socket and could not be measured.

Experience with the lossy socket shows that an interference reduction can be obtained with the use of lossy materials. However, the amount of the reduction obtained is limited by the volume of lossy material used and is frequency dependent. Little or no protection occurs at the lower frequencies (220 MHz), where devices are typically the most susceptible. Lossy materials may be useful in conjunction

Figure 6.1. 16--Pin Lossy Ferrite Socket

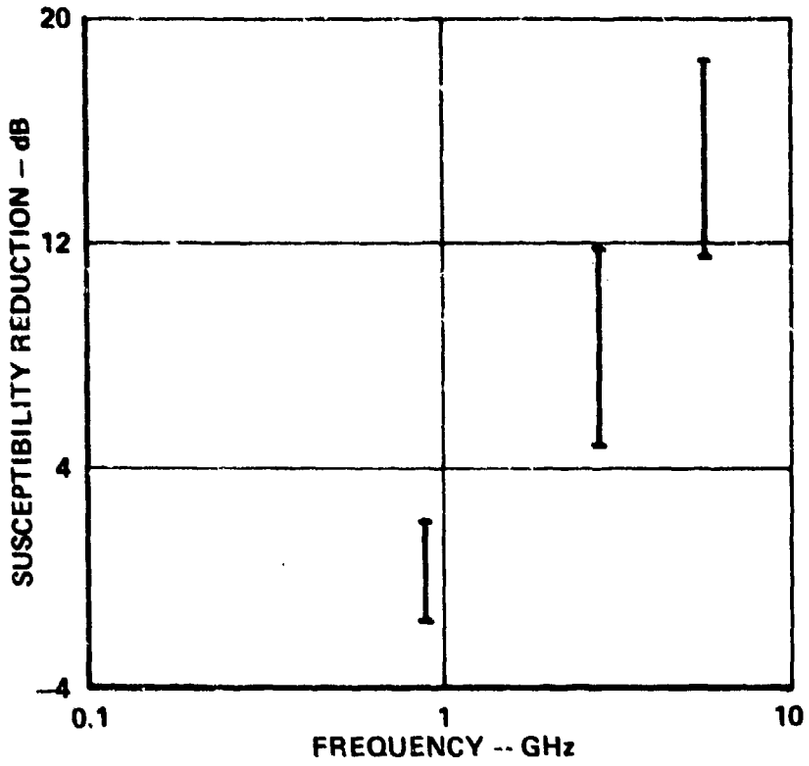


Figure 6.2. Protection from Lossy Ferrite Socket Measured for 4007, 7400, and 747 ICs

with other susceptibility reduction techniques (shielding, etc.) as part of a total system hardening plan.

6.3 Less Susceptible Circuit Designs

Several courses of action are available to the circuit designer to minimize interference effects in electronic equipment. These include using digital instead of analog circuitry, using high signal levels, avoiding the use of high speed semiconductors, and the use of common mode cancellation.

Often, significant interference reduction can be obtained by using digital instead of analog circuitry at those locations where RF is expected to be present. Digital circuitry has a higher interference immunity than analog circuitry. Small voltage or current offsets which may significantly alter an analog signal will not affect a digital signal until the offsets become large enough to induce state changes. Signals that originate in analog form, as from a sensor, must be carefully protected until they can be converted to digital form by an analog-to-digital converter.

The use of high signal levels will also minimize the probability of interference. In digital circuits, greater interference immunity will be obtained because larger voltage or current offsets will be required to cause state changes. In analog circuits, the percentage change in signal level for a given RF induced offset will be less if a circuit uses high signal levels.

If possible, use low speed semiconductor devices. Many semiconductors in use today are very fast, and are able to rectify signals at gigahertz frequencies. Where a circuit is designed for low frequency operation, the use of semiconductors capable of operating at high frequencies will increase the circuit's interference susceptibility. Unfortunately, many of the semiconductor devices which are built on modern integrated circuit chips are also very fast which makes them susceptible to high frequency energy. In most cases, the circuit designer does not have the option

of specifying integrated circuits containing significantly slower semiconductors.

The common mode cancellation properties of differential amplifiers may be used up through the VHF region to reduce the interference response of a circuit. If equal amounts RF power unter both inputs of a differential amplifier simultaneously then, in theory, equal rectification and equal offsets will occur at each input terminal, which will be cancelled out by the differential amplifier. An RF coupling device such as a shunt capacitor or a bifilar transformer can be used to ensure that equal RF levels exist at the two input terminals. Tests of op amps with a capacitor shunting the inputs have shown that roughly 3 to 10 dB of susceptibility reduction is obtained at 3 GHz.

Good circuit construction practices help minimize a circuit's susceptibility to RF energy. Minimizing the length of interconnect wiring and the use of shielded and twisted pair wire will reduce the amount of RF energy picked up. The use of filters, chokes, and ferrite beads can efficiently reduce the RF power reaching sensitive portions of the circuit.

REFERENCES

This section provides a list of the documents used as sources of information in preparation of this report. Reports referenced with a number of the form NXX-XXXXX are available through:

National Technical Information Service
U. S. Department of Commerce
Springfield, VA 22161.

Reports referenced with a number of the form AD-XXXXXXX are available through:

Defense Documentation Center
Cameron Station
Alexandria, VA 22314.

1. Design Handbook for Control of RF/Microwave Electromagnetic Effects, to be published by the Naval Surface Weapons Center, Dahlgren, Virginia.

2. "Integrated Circuit Electromagnetic Susceptibility Investigation - IC Susceptibility Handbook - Draft 1," McDonnell Douglas Astronautics Company, St. Louis, MDC E1515, 4 June 1976, N77-17383, AD-A029224.

3. "Integrated Circuit Electromagnetic Susceptibility Investigation - IC Susceptibility Handbook - Draft 2," McDonnell Douglas Astronautics Company, St. Louis, MDC E1669, 3 June 1977, N78-10392, AD-A043777.

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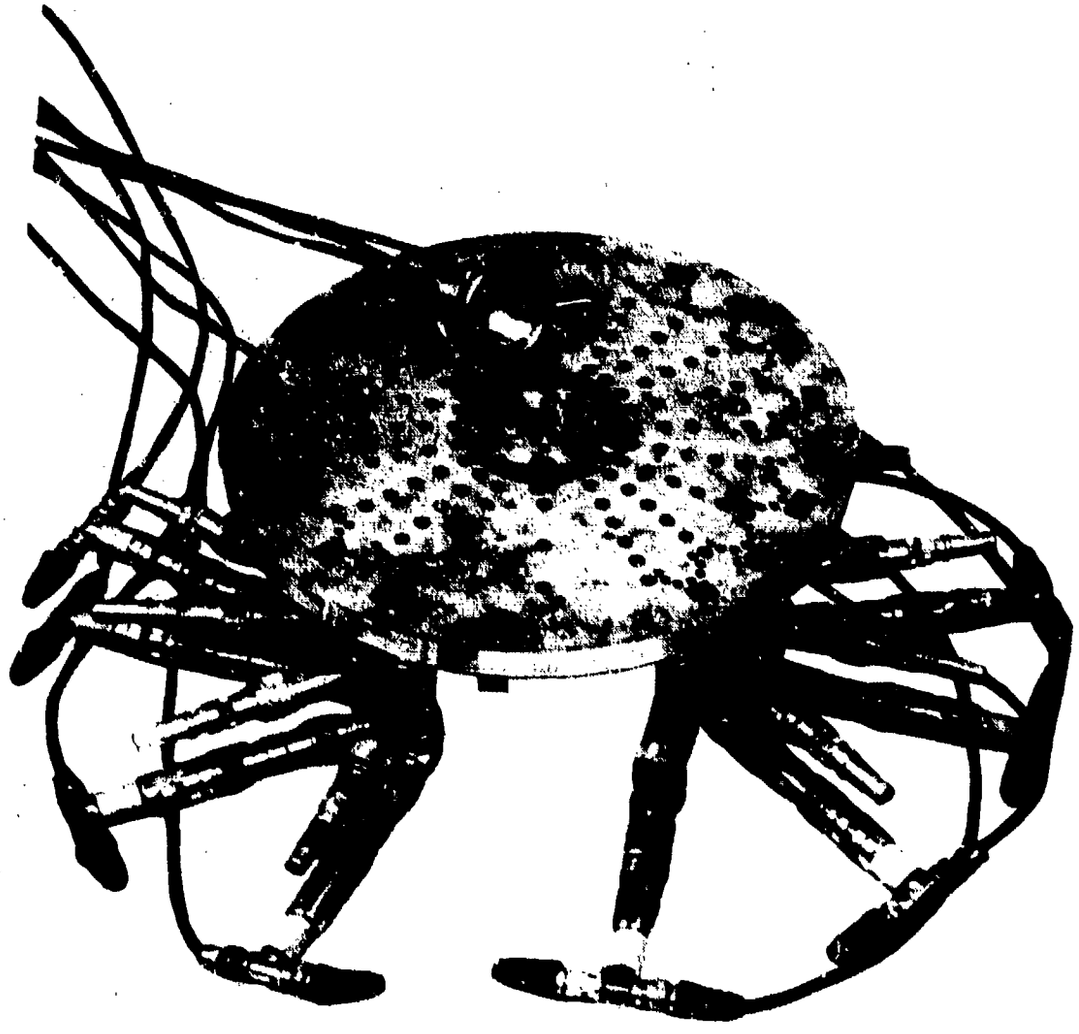
APPENDIX A

MEASUREMENT TECHNIQUES

The measurement of the RF susceptibility of integrated circuits is a complex task. Consideration of the number of types of IC's, the many operating conditions in which they are found, and the possible combinations of RF conditions to which they may be subjected (including frequency, modulation, power level, impedance, and RF entry location parameters) reveals that a large amount of testing is required for an accurate characterization of the RF susceptibility properties of integrated circuits. Additionally, each test must be meaningful and repeatable, and permanent documentation is desired for each test. To satisfy these requirements, special test techniques were developed. They include the development of special test fixtures and a computerized experiment control system, which are briefly described in this section. Reference 23 contains additional information on the measurement techniques that were used.

Special test fixtures were needed to perform in-depth tests of integrated circuits using microwave frequencies. Fixtures were built to accomodate several common integrated circuit package styles. Figures A.1 through A.6 illustrate the fixtures constructed for 16-pin dual in-line packages, 16-pin flatpacks, and 10-pin TO-5 packages. Stripline networks conduct signals from bias units located at the periphery of the test fixture to conventional IC sockets located in the center. A metal cap confines all electromagnetic energy within the test fixture so that radiation does not occur. Detailed drawings of the test fixtures are available from the U. S. Naval Surface Weapons Center (address inside front cover).

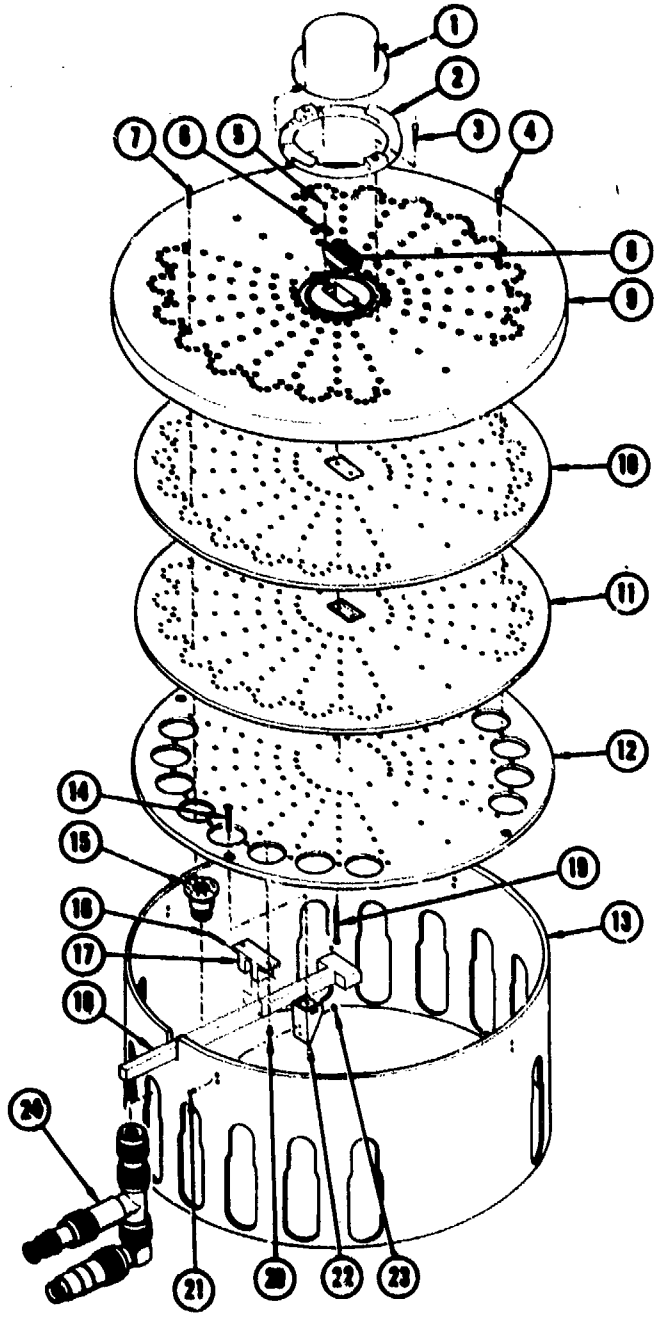
The bias units allow for independent adjustment of the microwave and video signals conducted into each IC terminal. The construction of a bias unit is illustrated in Figure A.7. The inset in Figure A.7 shows that the bias unit



(TEST FIXTURE SKIRT OMITTED FOR CLARITY)

Figure A.1. Dual In-Line Package Test Fixture

combines video and microwave lines into a single line. The video arm of the bias unit can be represented schematically by a series inductor and is capable of passing signals with risetimes as fast as 80 nanoseconds. The microwave arm is represented schematically by a series capacitor, and will conduct RF frequencies down to 100 MHz. The losses of the bias units and stripline sections are calibrated at five frequencies: 0.22, 0.91, 3.0, 5.6, and 9.1 GHz.



PARTS LIST		
ITEM NO.	NAME	NUMBER REQUIRED
1	COVER PLUG	1
2	SPRING LOADED HOLD DOWN	1
3	SCREW – 4-40 X 3/4	2
4	SCREW – 6-32 X 1/2	114
5	SCREW – 0-80 X 1/8	2
6	TAB	2
7	SCREW – 2-56 X 1/2	112
8	16 PIN DIP SOCKET	1
9	TOP COVER PLATE (DIP)	1
10	TOP STRIP LINE BOARD (DIP)	1
11	BOTTOM STRIP LINE BOARD (DIP)	1
12	BOTTOM COVER PLATE (DIP)	1
13	TEST FIXTURE SKIRT	1
14	SCREW 6-32 X 3/4	4
15	STRIPLINE LAUNCHER	16
16	EJECTOR PIVOT PIN	1
17	EJECTOR PIVOT	1
18	EJECTOR ARM	1
19	EJECTON PIN	2
20	SCREW 4-40 X 1 8	2
21	SCREW 2-56 X 1/4	8
22	FASTENER	4
23	NUT 2-56	8
24	BIAS UNIT	16

Figure A.2. Dual In--Line Package Test Fixture (Exploded View)

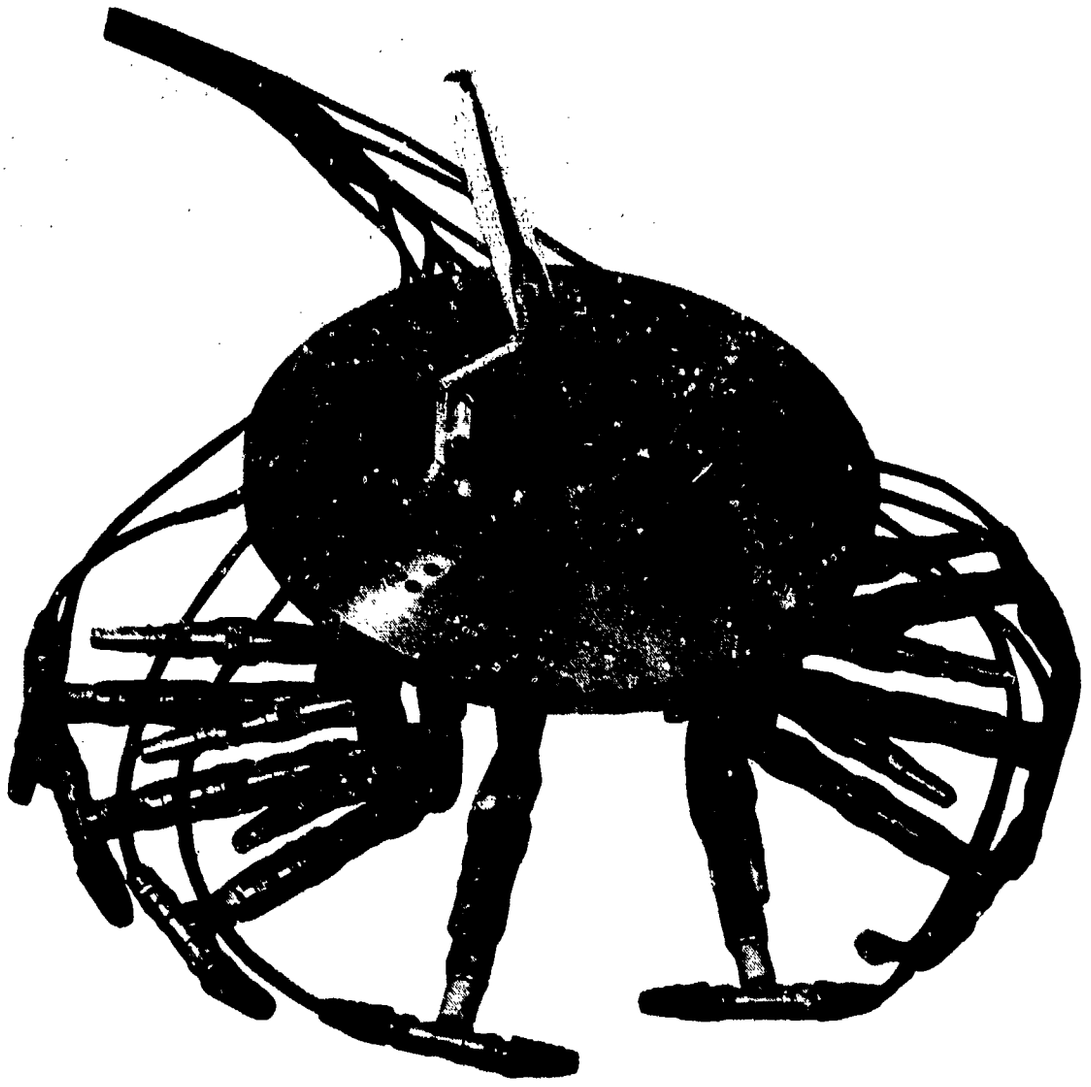


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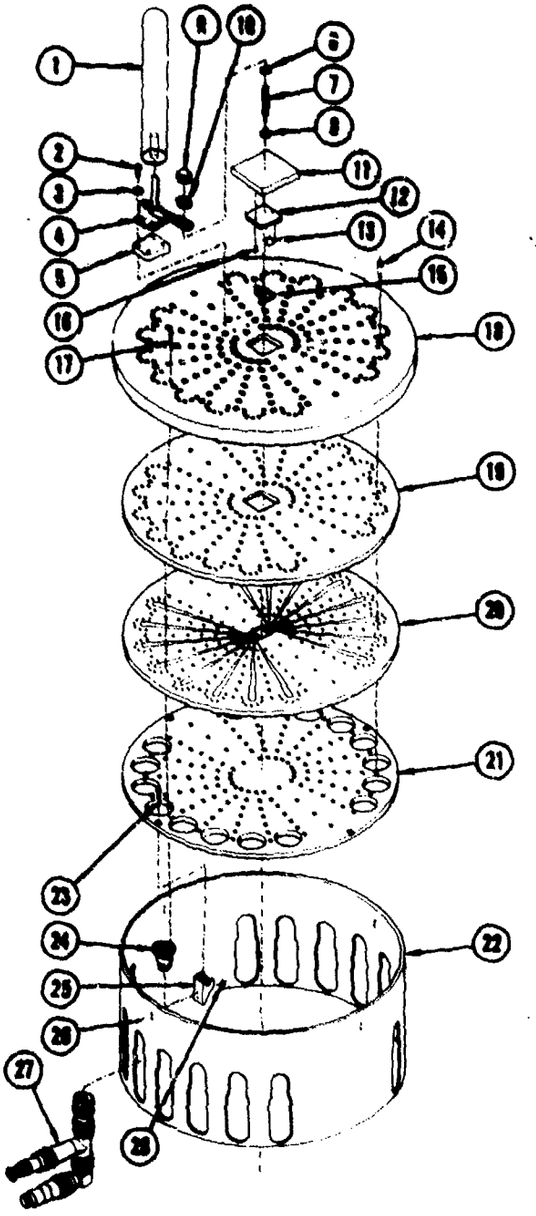
Figure A.3. Flat Pack Package Test Fixture

The bias units allow the device to be biased in an actual operating condition, including supply voltage, input source and output loads. Often the input and output voltages and currents are supplied through active devices. For example, in the case of logic gates, the input voltage to the device under test may be supplied by a gate (located outside the test fixture), and the device under test may drive another gate at its output to simulate the conditions seen by the IC in a digital circuit.



PARTS LIST		
ITEM NO.	NAME	NUMBER REQUIRED
1	PLASTIC HANDLE	1
2	SCREW 8-32 x 0.375 ROUND HEAD	4
3	WASHER FOR 8-32 SCREW	4
4	TOGGLE CLAMP	1
5	TOGGLE CLAMP BASE	1
6	NUT 10-24	1
7	COVER PLUG PRESSURE SCREW	1
8	COVER PLUG PRESSURE FOOT	1
9	CAP NUT	1
10	NUT	1
11	COVER PLUG TOP	1
12	COVER PLUG DIELECTRIC INSERT	1
13	NON CONDUCTIVE COMPRESSIVE RUBBER FOR IC LEAD CONNECTION	2
14	SCREW 6-32 X 1 1/2	114
15	IC LEAD LOCATOR PLUG	1
16	SCREW 8-80 X 1/4 FLAT HEAD	2
17	SCREW 2-56 X 1 1/2	112
18	TOP COVER PLATE (FLAT PACK)	1
19	TOP STRIP LINE BOARD (FLAT PACK)	1
20	BOTTOM STRIP LINE BOARD (FLAT PACK)	1
21	BOTTOM COVER PLATE (FLAT PACK)	1
22	TEST FIXTURE SKIRT	1
23	SCREW 6-32 X 1 1/2	4
24	STRIP LINE LAUNCHER	16
25	FASTENER	4
26	SCREW 2-56 X 1/4	16
27	BIAS UNIT	16
28	NUT 2-56	16

Figure A.4. Flat Pack Package Test Fixture (Exploded View)

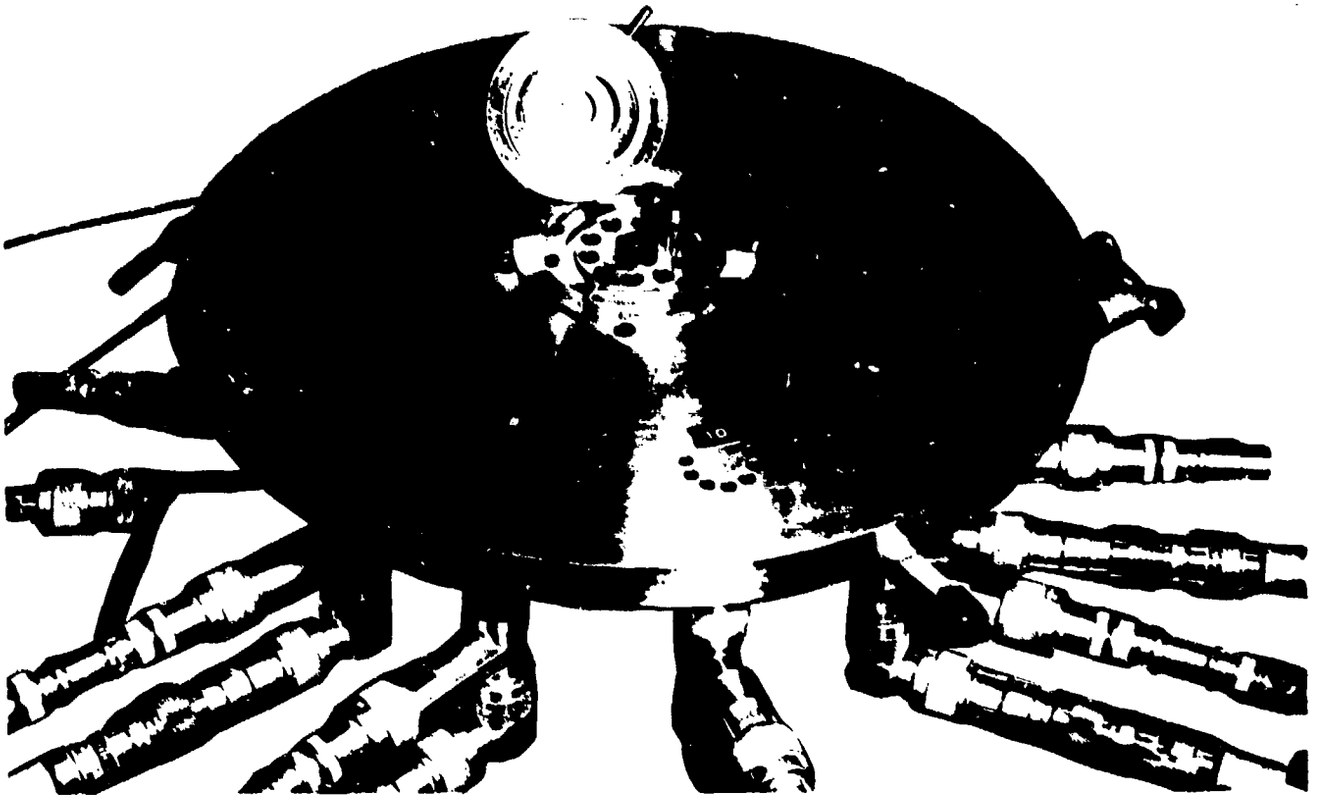


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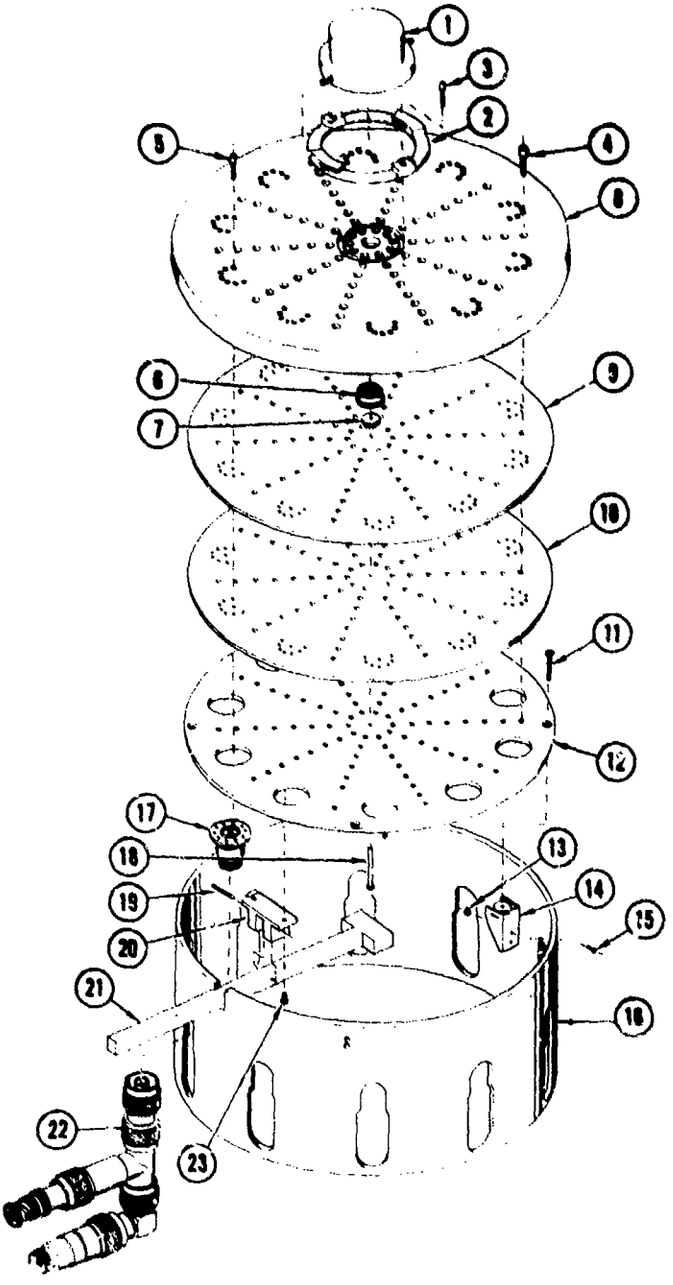
Figure A.5. TO–5 Package Test Fixture

During a test, RF is conducted into a single terminal via the RF line of the appropriate bias unit. A reflectometer consisting of directional couplers and calibrated crystal detectors is used to monitor the incident and reflected powers at the RF input port. Calibrated crystal detectors attached to the RF arm of all remaining bias units measure the RF power transmitted through the IC and test fixture. It is possible to estimate the RF power absorbed in the test device from measurements of the incident, reflected, and transmitted power levels.

Due to the large amount of testing required to determine the susceptibility of many devices at 5 frequencies and different RF input terminal combinations, and the large amount of data generated in each test, an automated test setup was used. A minicomputer controlled the experiments. Computer peripherals include an A-D



PARTS LIST		
ITEM NO.	NAME	NUMBER REQUIRED
1	COVER PLUG	1
2	SPRING LOADED HOLD DOWN	1
3	SCREW 4-40 X 3 4	2
4	SCREW 6-32 X 1 2	80
5	SCREW 2-56 X 1/2	70
6	TO-5 TEST SOCKET	1
7	TO-5 SOCKET	1
8	TOP COVER PLATE (TO-5)	1
9	TOP STRIPLINE BOARD (TO-5)	1
10	BOTTOM STRIPLINE BOARD (TO-5)	1
11	SCREW 6-32 X 1 2	4
12	BOTTOM COVER PLATE (TO-5)	1
13	NUT 2-56	8
14	FASTENER	4
15	SCREW 2-56 X 1 4	8
16	TEST FIXTURE SKIRT	1
17	STRIPLINE LAUNCHER	10
18	EJECTOR PIN	1
19	EJECTOR PIVOT PIN	1
20	EJECTOR PIVOT	1
21	EJECTOR ARM	1
22	BIAS UNIT	10
23	SCREW 4-40 X 1 8	2

Figure A.6. TO-5 Package Test Fixture (Exploded View)

subsystem for measuring IC and crystal voltages, a D-A subsystem to control the RF parameters and certain device dc levels, a printer and plotter to obtain a permanent hard-copy record of the test, and magnetic tape unit for storage of test

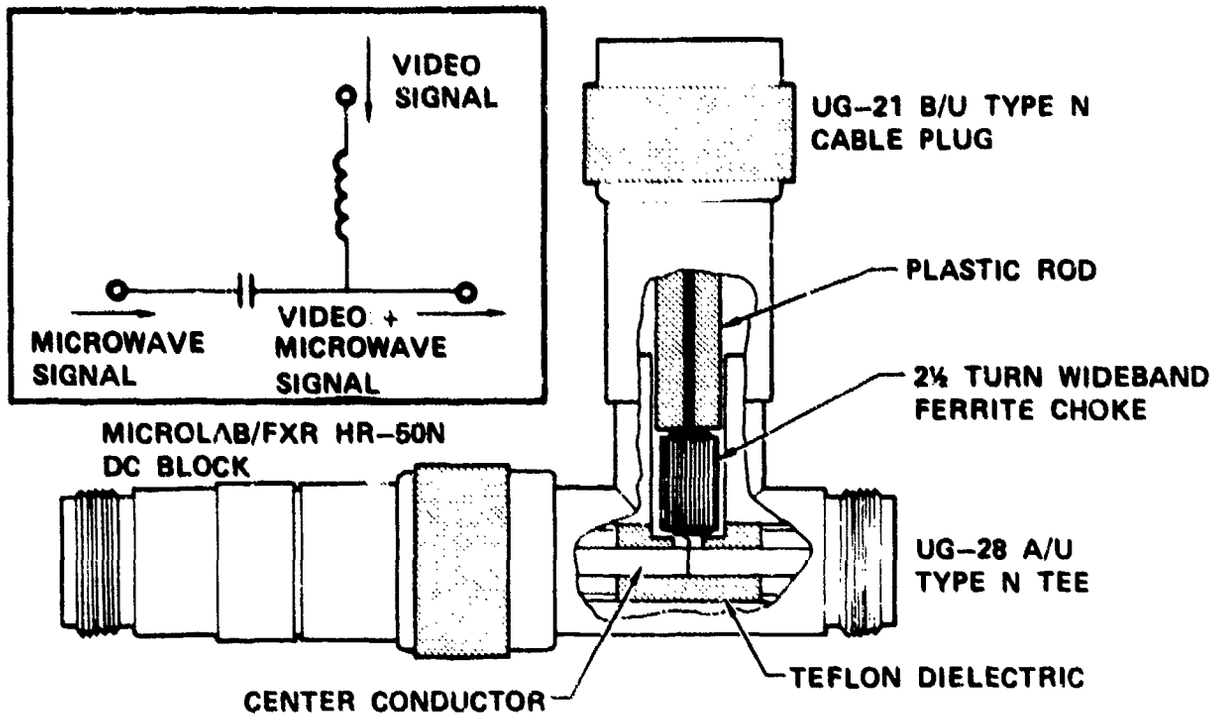


Figure A.7. Microwave Bias Unit

data for later analysis. Computer programs, written in FORTRAN IV, control the test by instructing the computer to establish the test conditions, control the RF signal level, and read the crystal and device voltages. The programs then apply calibration factors, analyze the data for specific effects, and print and store on tape a permanent record of the test. Figure A.8 is a photograph of the automated measurement system.

For interference testing, CW microwave signals were used. Figure A.9 shows a block diagram of the automated measurement system used for interference measurements. For high power damage testing, pulsed RF signals were used. To provide capability for single pulse testing, peak detectors were added to hold the maximum crystal detector voltages produced by the RF pulse until they were read by the computer. Figure A.10 shows a block diagram of the high power pulsed RF test setup.

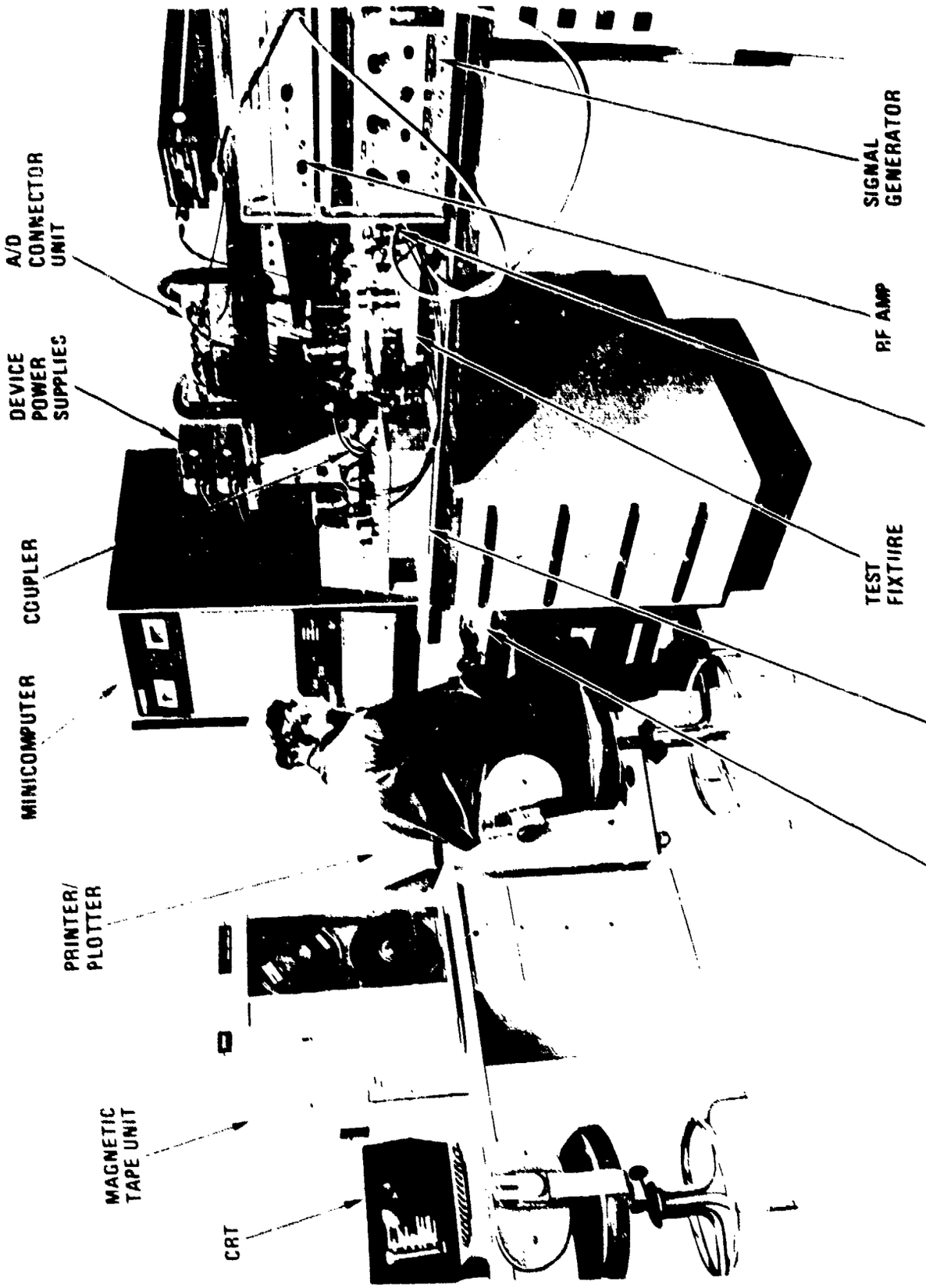


Figure A.8. IC Susceptibility Measurement System with Minicomputer

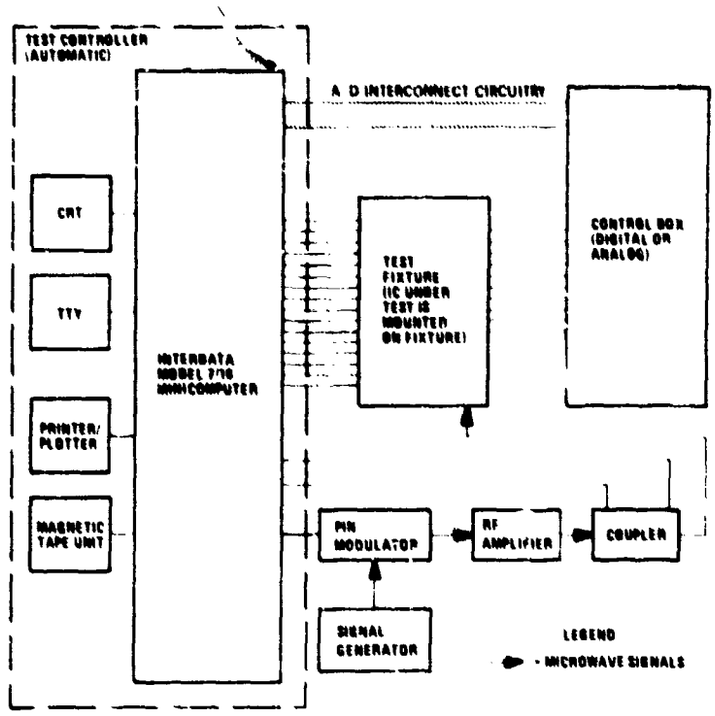


Figure A.9. Block Diagram of IC Interference Susceptibility Measurement System with Minicomputer

A few difficulties were encountered using the measurement techniques described here, primarily related to the determination of the RF power absorbed in the device. The equipment, including fixtures, couplers, and detectors, was calibrated using single frequencies, but the nonlinear nature of semiconductor devices leads to the generation of harmonics, the relative levels of which depend on the power level. The signal seen by the detectors thus contains many different frequencies, and determination of the actual RF power level based on calibrations at single frequencies is unreliable. Where reflection coefficients are high, or where transmission through the chip is large, the absorbed power calculation often involves finding the difference of large numbers resulting in a small value with a relatively high uncertainty. In the pulse testing, device impedances often change abruptly at the moment of failure. The signals recorded by the peak detectors may occur at different times during the RF pulse, and the sum of the transmitted and reflected

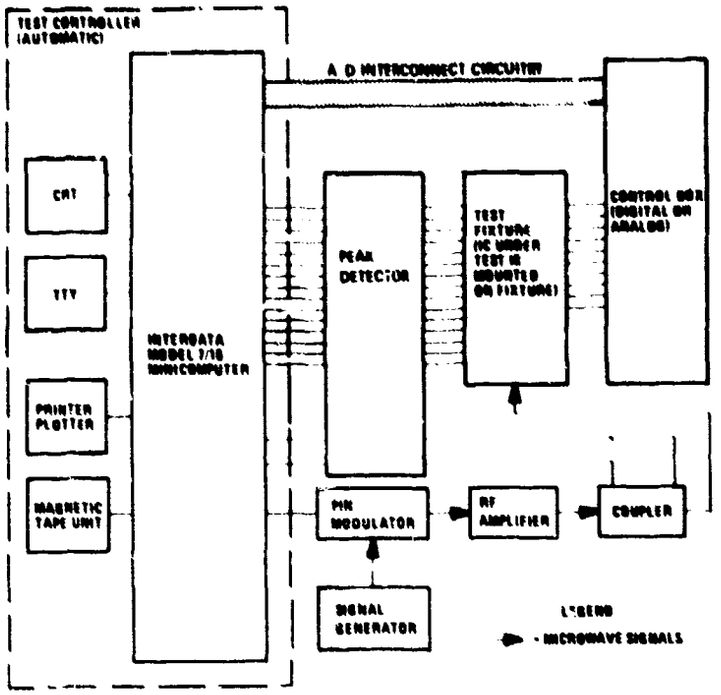


Figure A. 10. Block Diagram of IC Pulse Susceptibility Measurement System with Minicomputer

powers may be greater than the incident power level. This problem could be circumvented by using other measurement schemes, such as gated sample and hold circuitry or storage oscilloscopes.

The measurement system described here was intended as a research tool, providing much capability and speed for investigating the susceptibilities of a large number of devices and for obtaining an understanding of the basic physical processes involved. However, RF susceptibilities of IC's could be measured with a much less elaborate system. Simpler and less expensive test fixtures could be built that retain many of the basic features as the ones described here. A nonautomated system would be adequate to conduct limited susceptibility tests on integrated circuits.

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The objective of this handbook is to provide system designers with integrated circuit (IC) susceptibility information in terms of microwave signals. This is the final draft of the IC Handbook. The first and second drafts of the IC Handbook were reviewed by potential users, and their comments and suggestions have been incorporated where possible. The data in this handbook includes interference and damage susceptibility levels for digital and linear ICs. Actual test data is included when available. Modeling techniques are

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presented for the determination of device susceptibilities where no test data is available. The handbook explains an electromagnetic vulnerability (EMV) hardening approach for electronic systems. Coupling and shielding considerations are discussed. Susceptibility reduction techniques such as component screening, the use of lossy materials, and less susceptible circuit designs are also discussed. The handbook includes a description of the automated measurement system used to measure and analyze the IC susceptibility data.

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